KEYSIGHT WORLD 2019

Designing Switched-Mode Power Supplies in the High di/dt Era

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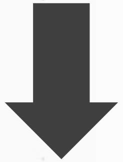
Trends in Switched-mode Power Supplies (SMPSs)

Customer Demands:

- **Smaller size**
- **Lighter weight**

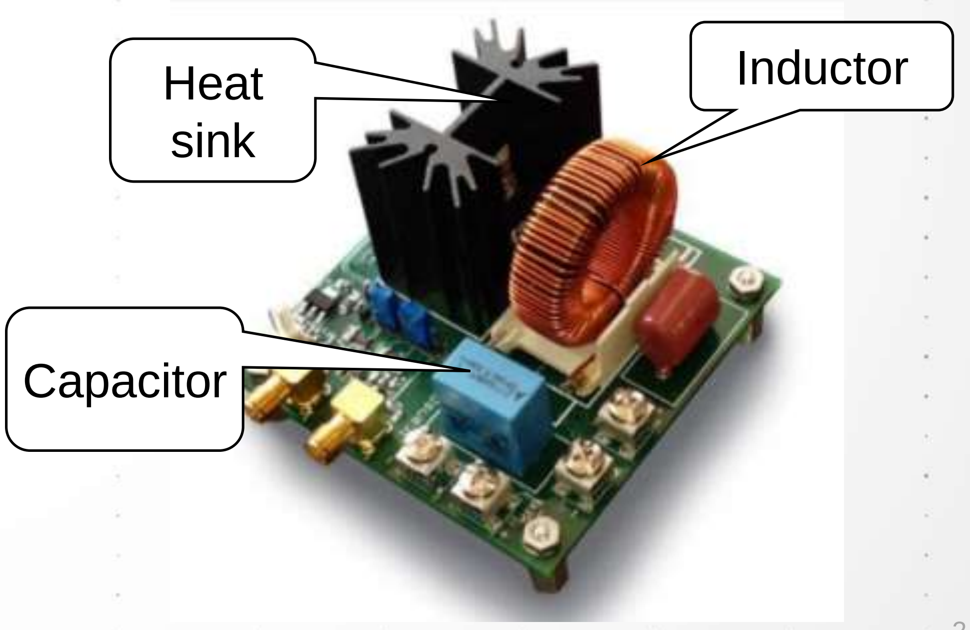


- **Higher switching speed (high di/ft)**
- **New technologies (accurate modeling)**

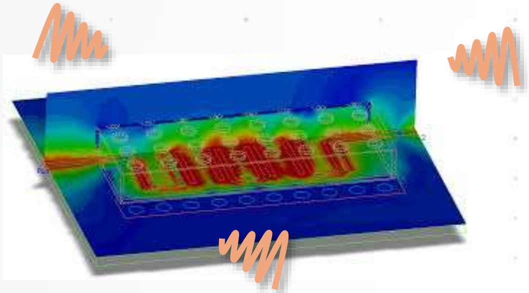
A magical shrinking machine doesn't exist!

Impact:

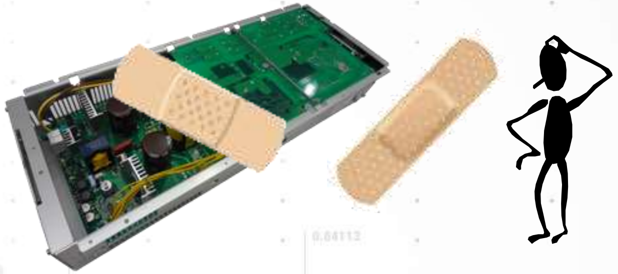
- **Performance**
- **Reliability**
- **Development/time to market costs**



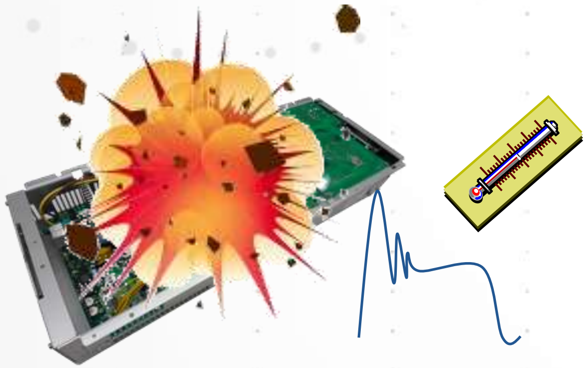
Challenges in power circuit design



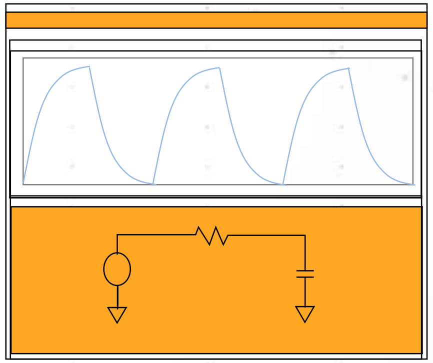
High switching frequency along with high frequency components in waveform causes unexpected EMI



High switching frequency and associated surge/ringing causes malfunction



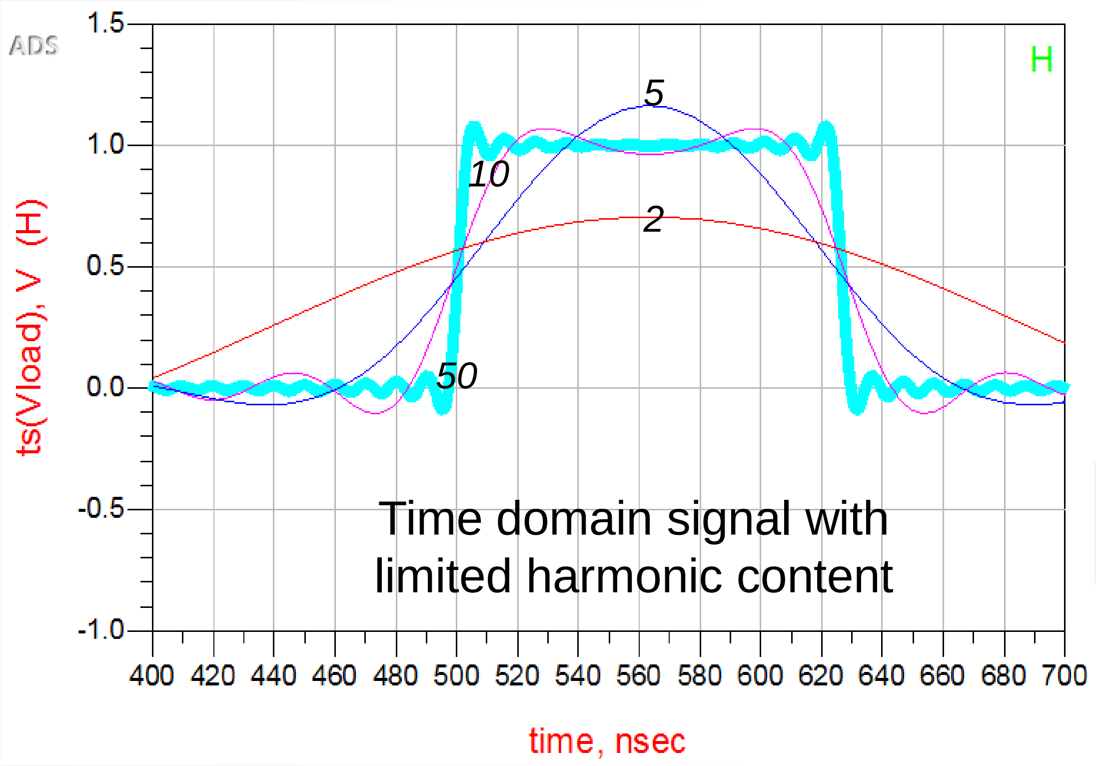
Prototype circuit explosion due to unexpected surge



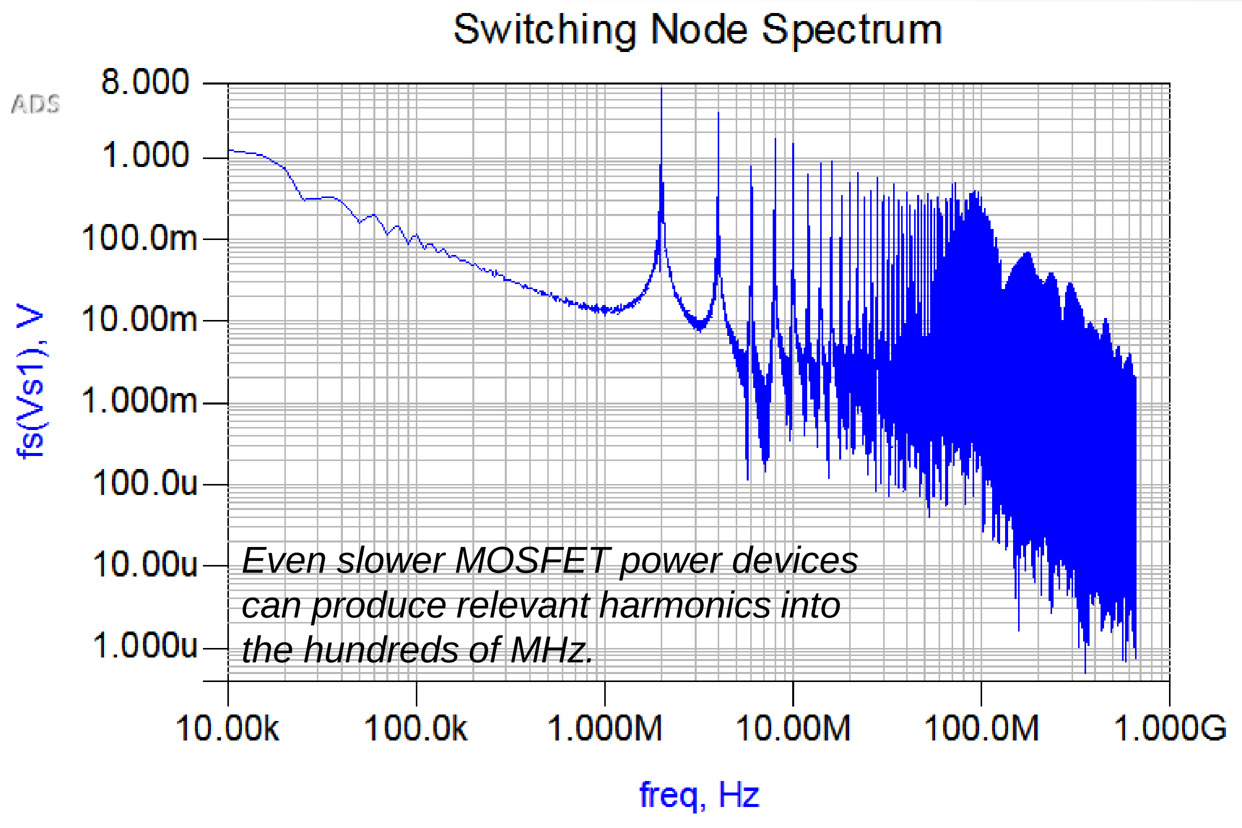
Lack of power circuit simulation tool. Conventional tool may work for low frequency circuit but not for WBG device circuit

High Speed Power Converter Challenge

THINKING IN THE FREQUENCY DOMAIN

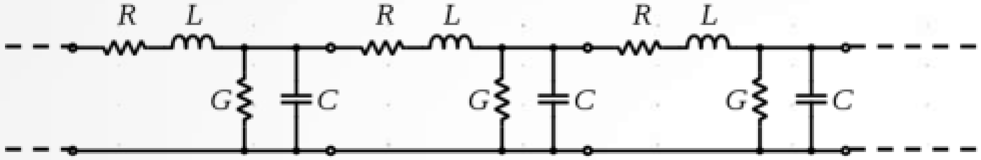


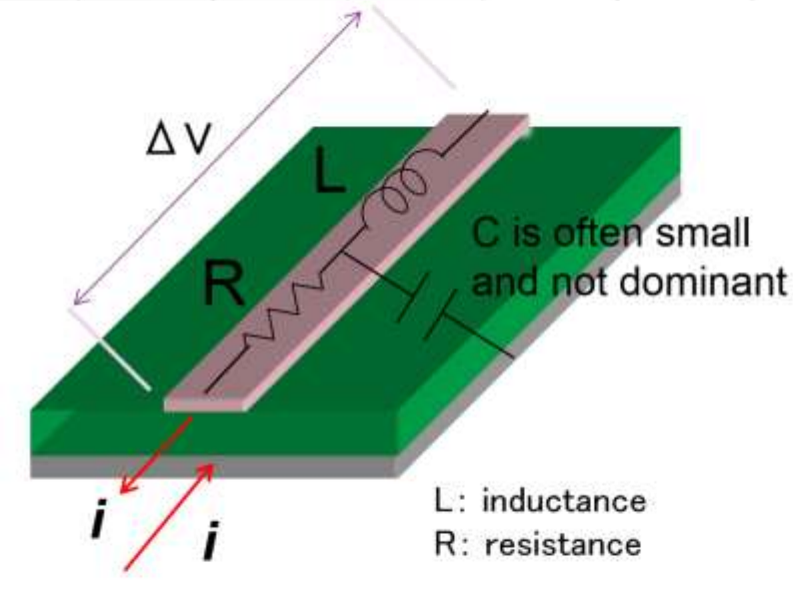
Time domain signal with limited harmonic content


Switching Node Spectrum

Even slower MOSFET power devices can produce relevant harmonics into the hundreds of MHz.

High speed power converters have relevant energy in the multi-GHz range!

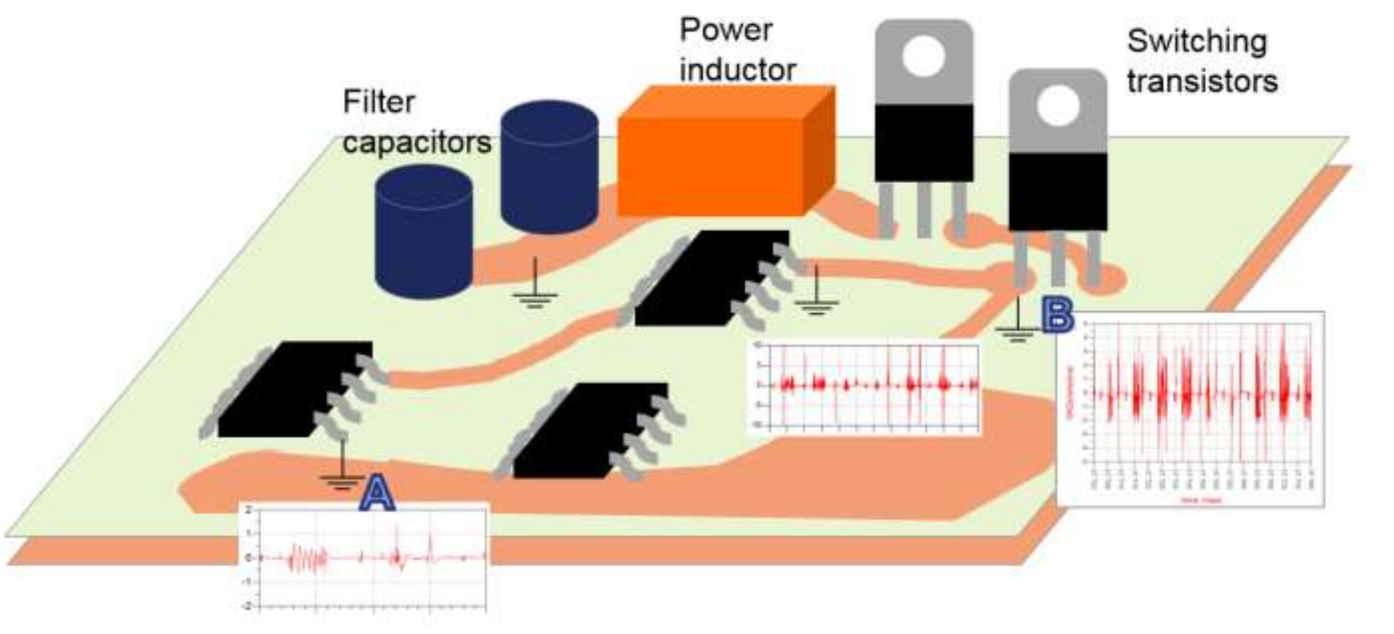




C is often small and not dominant

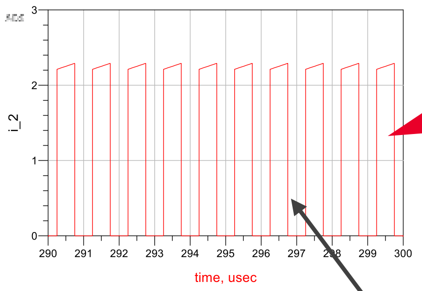
L: inductance
R: resistance

$$\Delta V = Ri + L\frac{di}{dt}$$



Switched-Mode Power Supply (SMPS)

SIMPLE EXAMPLE: HARD-SWITCHED BUCK CONVERTER



Rectangle wave duty cycle, D

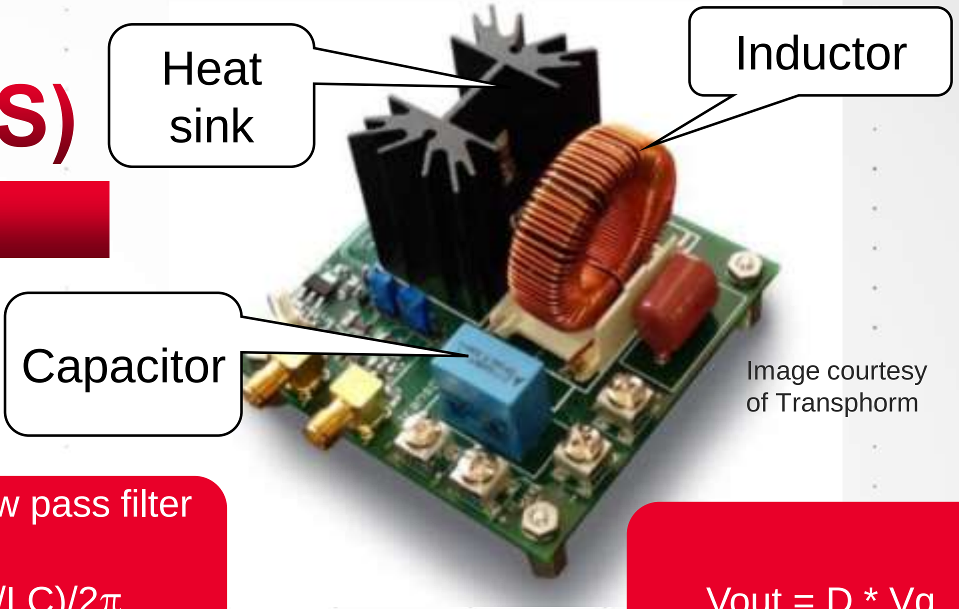
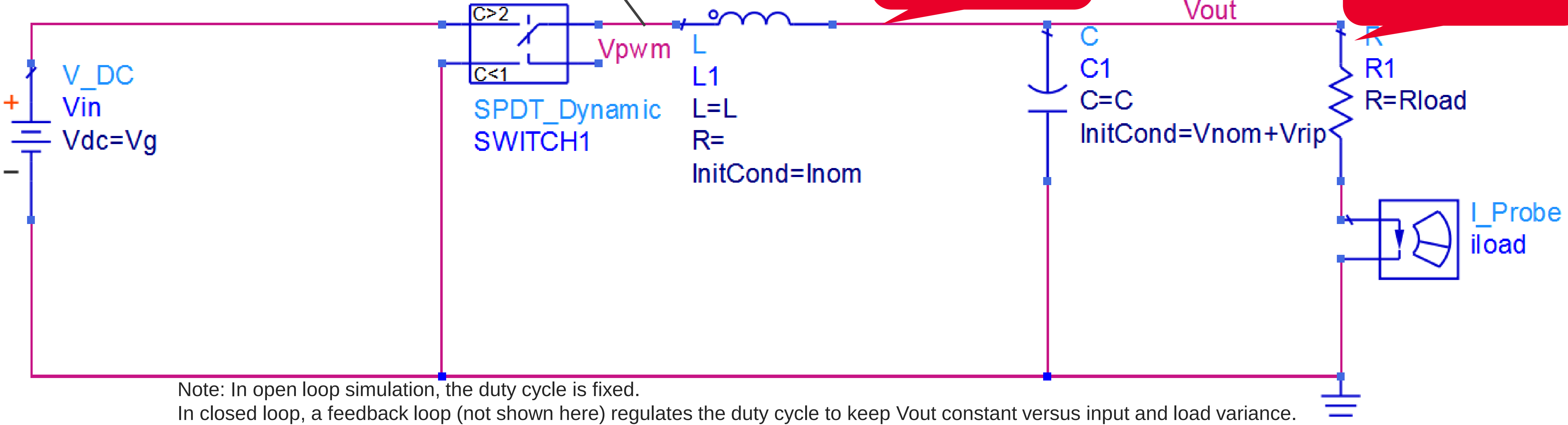


Image courtesy of Transphorm

LC low pass filter $f_{knee} = \sqrt{1/LC}/2\pi$

Vout = D * Vg

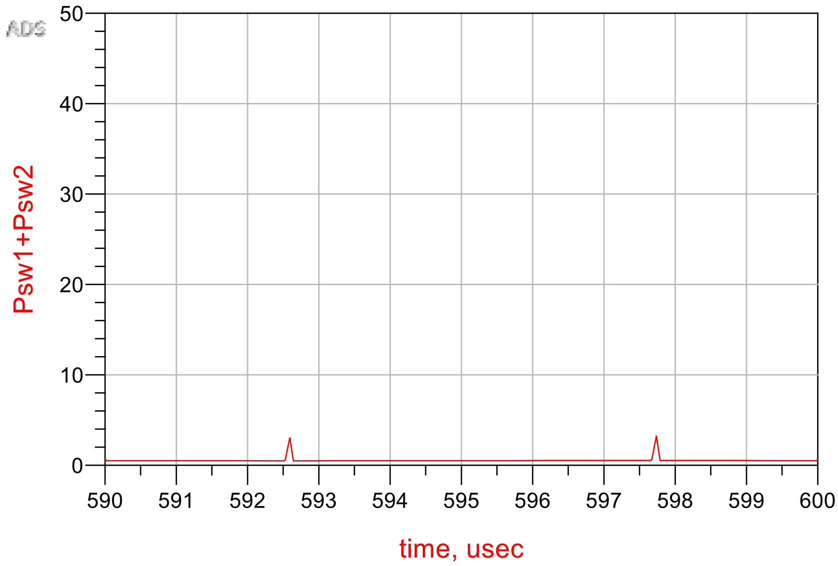


Note: In open loop simulation, the duty cycle is fixed.
In closed loop, a feedback loop (not shown here) regulates the duty cycle to keep Vout constant versus input and load variance.

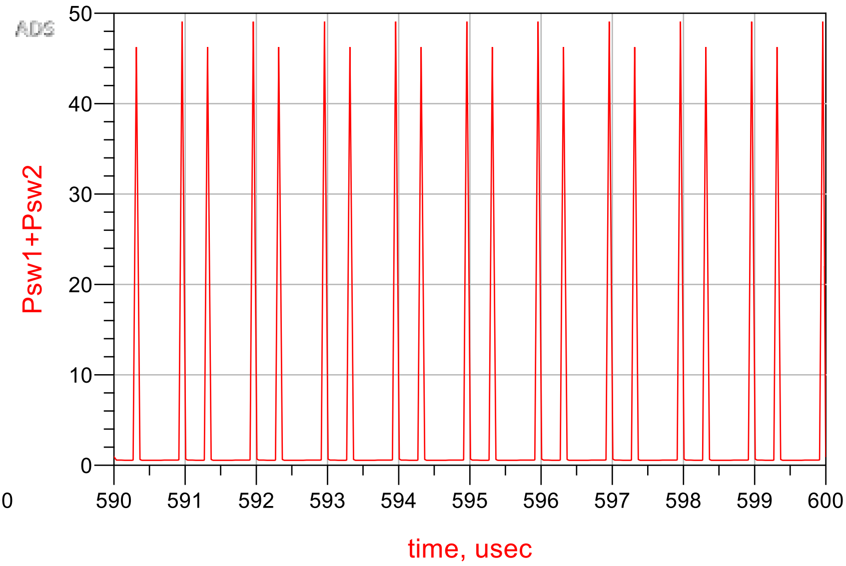
Higher Frequency Can Lead to Higher Switching Loss

UNLESS THE EDGE SPEED IS INCREASED AS WELL

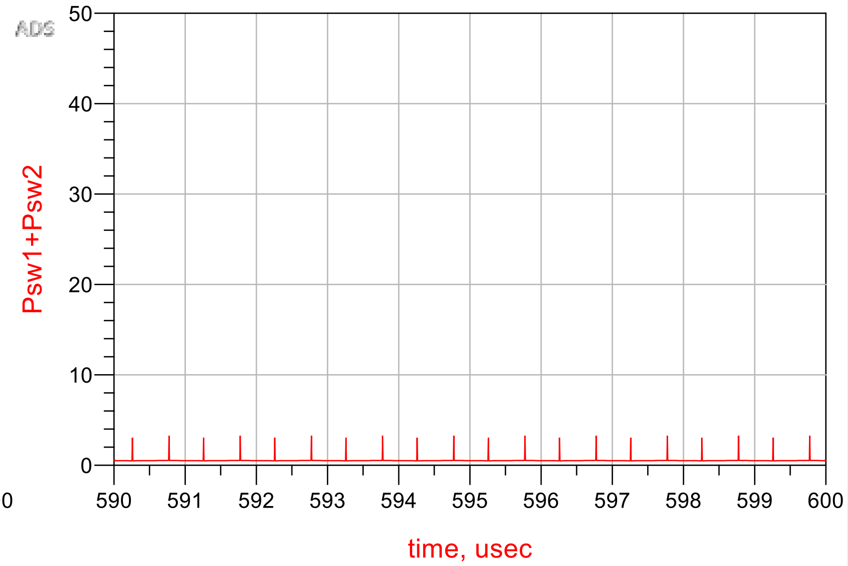
Low frequency
Slow edges
Switching loss 3.5%



Higher frequency
Same slow edges
Switching loss 15.3%

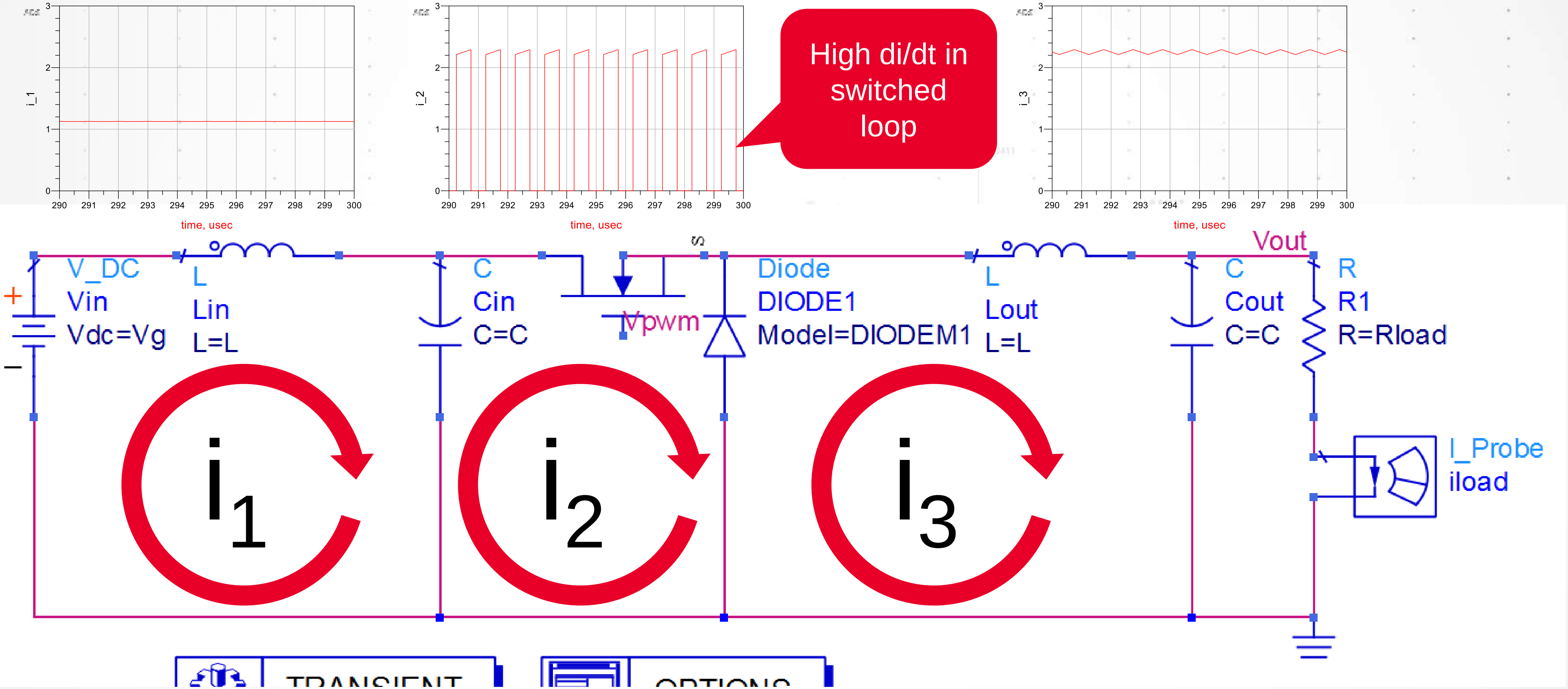


Higher frequency
Faster edges
Switching loss 3.3%



If you want to *reduce* switching loss, you have to improve the edge speed *even more dramatically* than improving the switching frequency

Current Loops: Schematic View



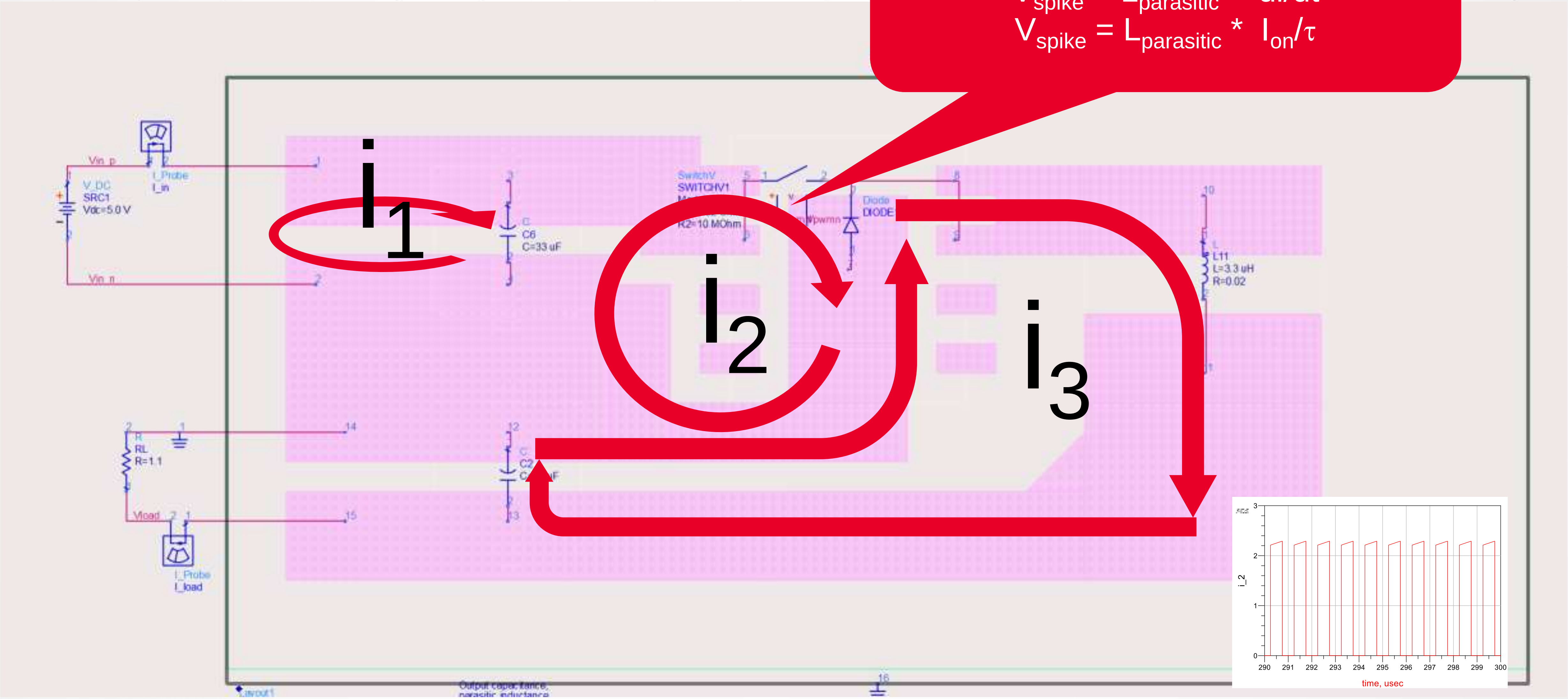
High di/dt in switched loop

Current Loops: Layout View

When does the layout of the switched loop become important?

$$V_{spike} = L_{parasitic} * di/dt$$

$$V_{spike} = L_{parasitic} * I_{on}/\tau$$



$$V_{spike} = L_{parasitic} \frac{I_{on}}{\tau}$$

Definition of inductance
Linear ramp di/dt

$$\frac{V_{spike}}{V_{off}} = L_{parasitic} \frac{I_{on}}{\tau V_{off}}$$

Divide both sides by Voff

$$10\% = L_{10\%} \frac{I_{on}}{\tau V_{off}}$$

What inductance will give us a overstress spike that is, say, 10% of Voff?

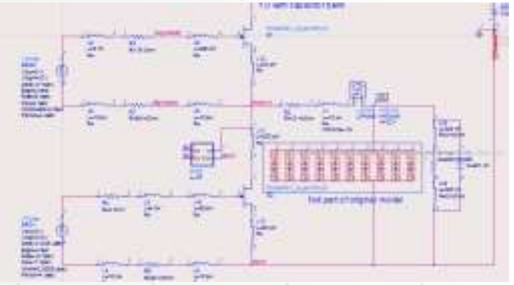
$$L_{10\%} = \frac{0.1 \tau V_{off}}{I_{on}}$$

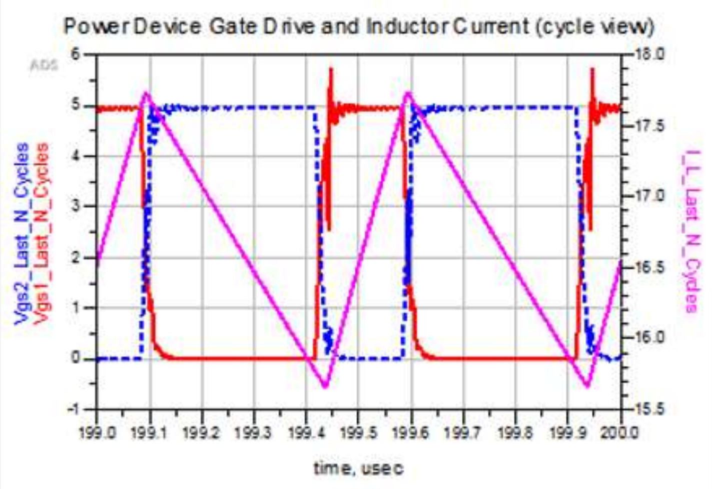
Rearrange, plug in some numbers
10 ns, 20V, 4A answer is 5 nH
Few mm of wire is 5 nH!

Traditional Low Speed Design Approach

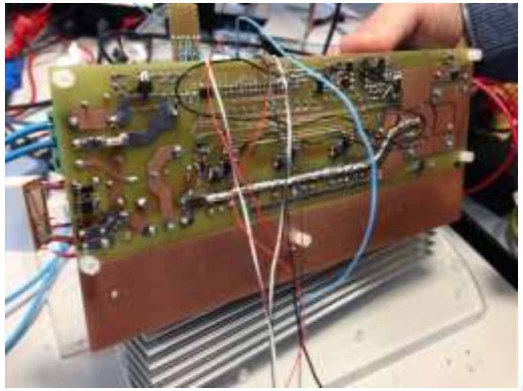
PRE-LAYOUT SPICE, THEN "CUT AND TRY"

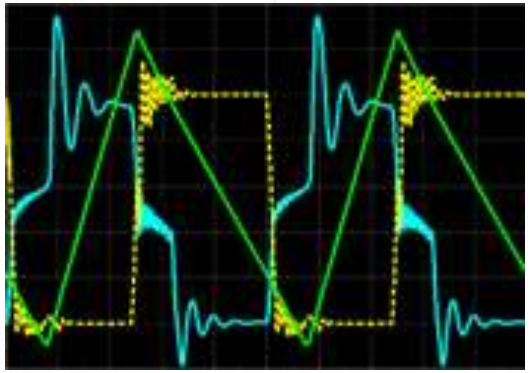
Pre-layout schematic
SPICE simulation:
"Best Case" performance





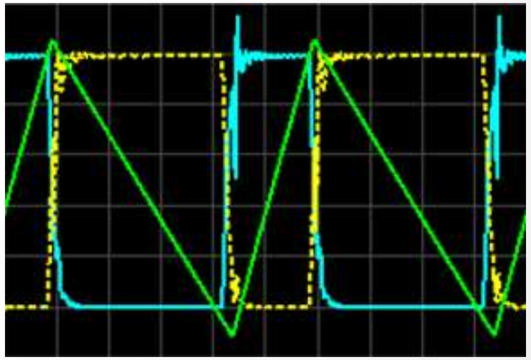
First prototype has some excess ringing. Cut-and-try until "best case" approached





2-6 spins
$6k-$60k/spin
3-8 weeks slip/spin

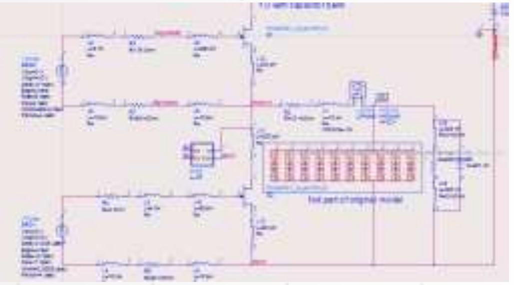
Image courtesy of ST Microelectronics

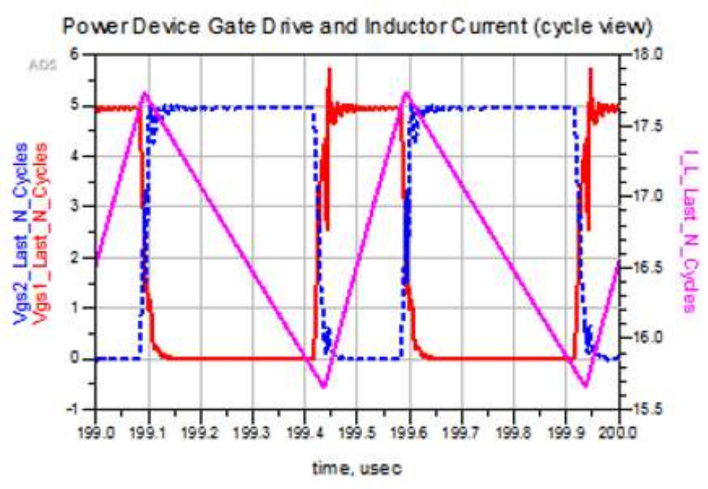


Traditional Design Approach Applied to High Speed

PRE-LAYOUT SPICE, THEN "CUT AND TRY"

Pre-layout schematic
SPICE simulation:
"Best Case" performance





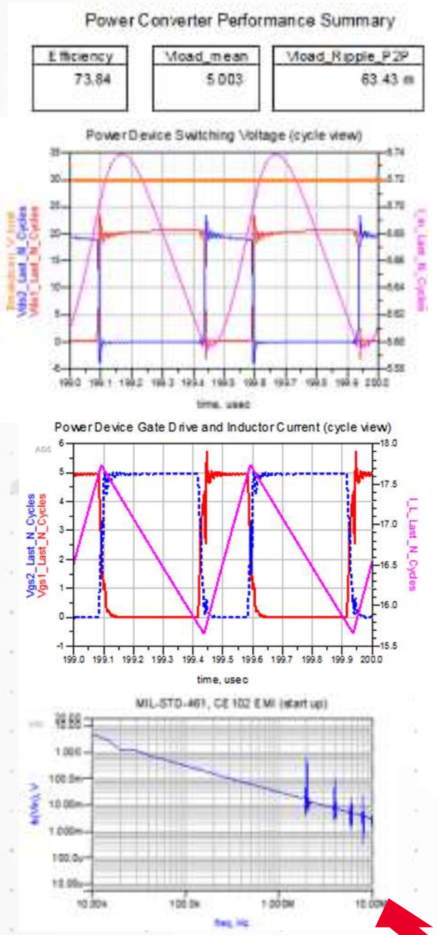
First prototype has destructive failure.

What next?

A suggested Design Approach

IDENTIFY AND FIX PROBLEMS BEFORE FABRICATION

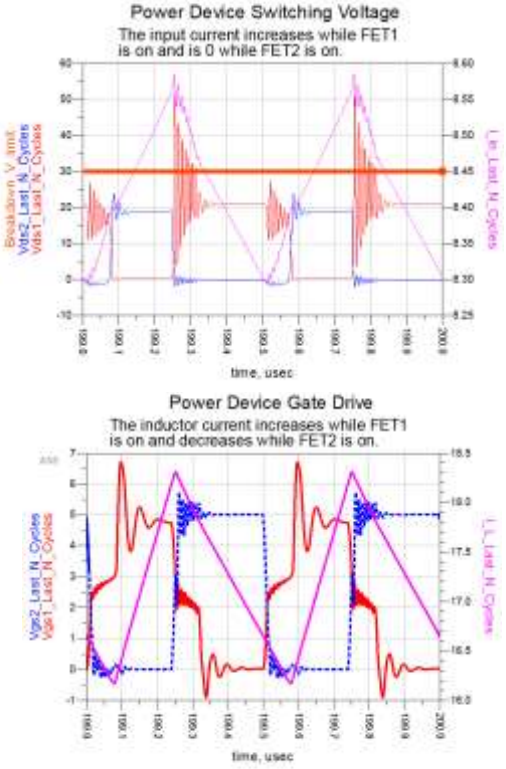
Schematic Only Simulation (Best Case)



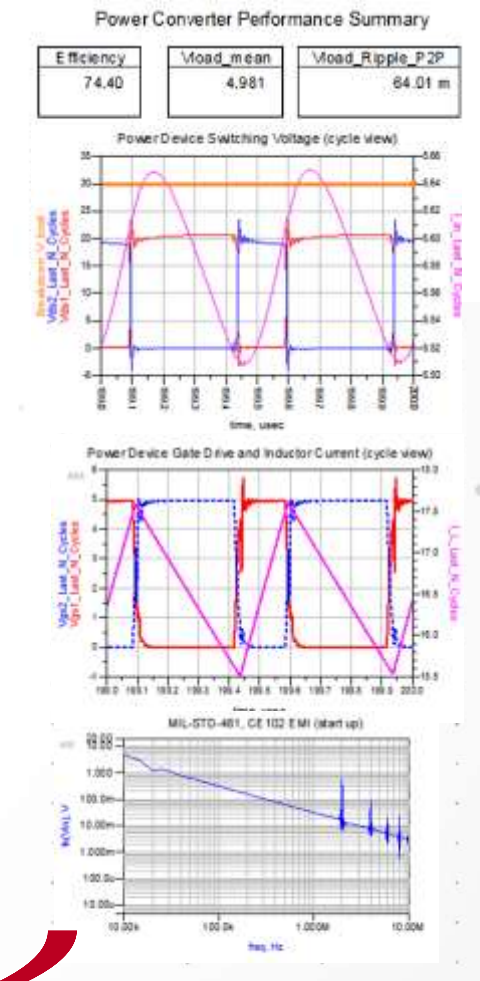
Power Converter Performance Summary

Efficiency	Vload_mean	Vload_Ripple_P2P
73.84	5.003	63.43 m

Identify & Fix Physical Design Issues with EM



Final EM Verification



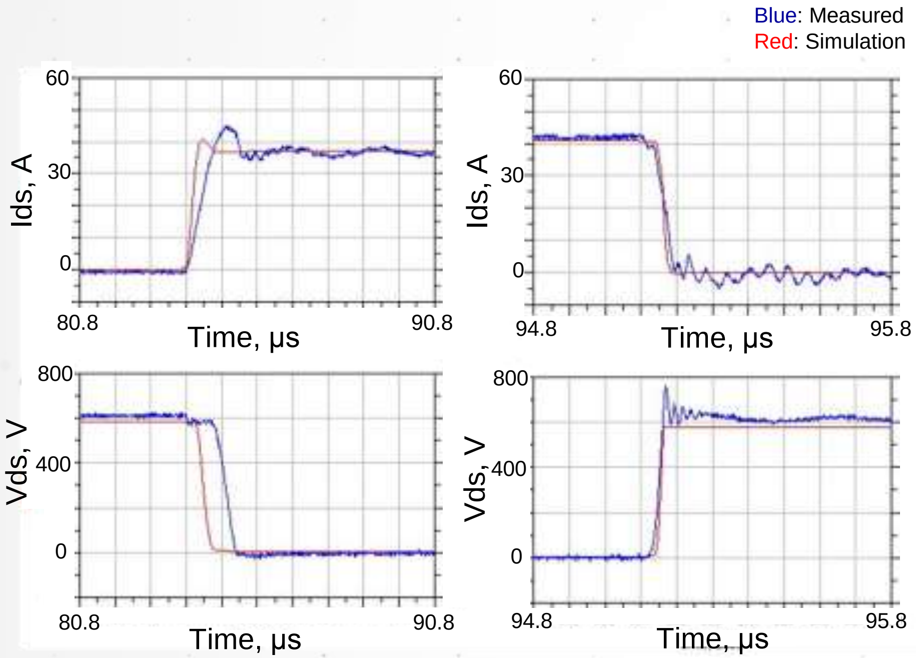
Power Converter Performance Summary

Efficiency	Vload_mean	Vload_Ripple_P2P
74.40	4.981	64.01 m

Restore Performance

Conventional simulation vs. New Keysight simulation method

Simulation with a conventional model

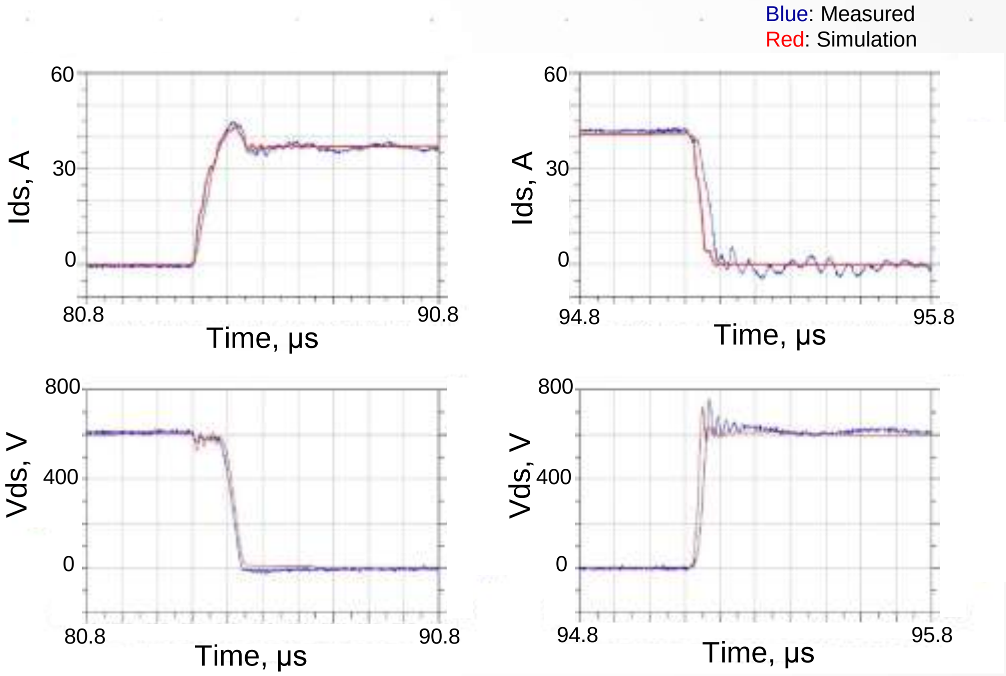


Waveforms don't match.

- Ringing/overshoot are not simulated (flat line)
- Timing deviation
- Slew rate deviation

Exact waveform match is critical for noise calculation as waveform contains high frequency components

Simulation with the Keysight math model



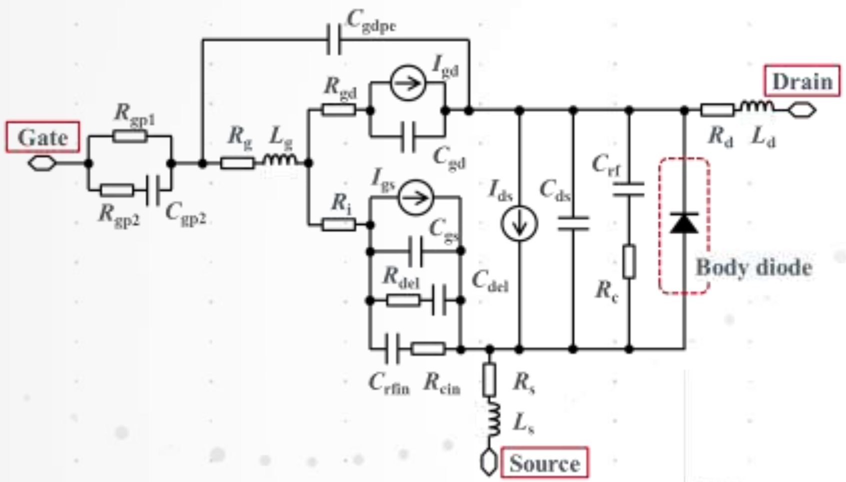
Excellent matching between simulation and measurement

Source: "Measurement Methodology for Accurate Modeling of SiC MOSFET Switching Behavior over Wide Voltage and Current Ranges", H. Sakairi, et. al., IEEE Trans on Power Electronics early access,

What makes this improvement?

What are different? (1)

DEVICE MODEL



Added body diode to better fit to SiC

$$\tanh\left(\left(\text{Lambda1} \times \tanh\left(1 + \text{Lambda2} \times V_{gs}\right)\right) \times V_{ds}\right)$$

Added Vgs, Vds dependent parameter to drain current equation to better represent unsaturated drain current

$$\begin{aligned} Q_{gs} \\ &= \left(C_{gspi} + C_{gs0} \times \tanh 02\right) \\ &+ \left(C_{gspi} + \left(C_{gs0} \times \tanh 01 + C_{gs0i} \times \tanh 1i\right) \times \tanh 02\right) \end{aligned}$$

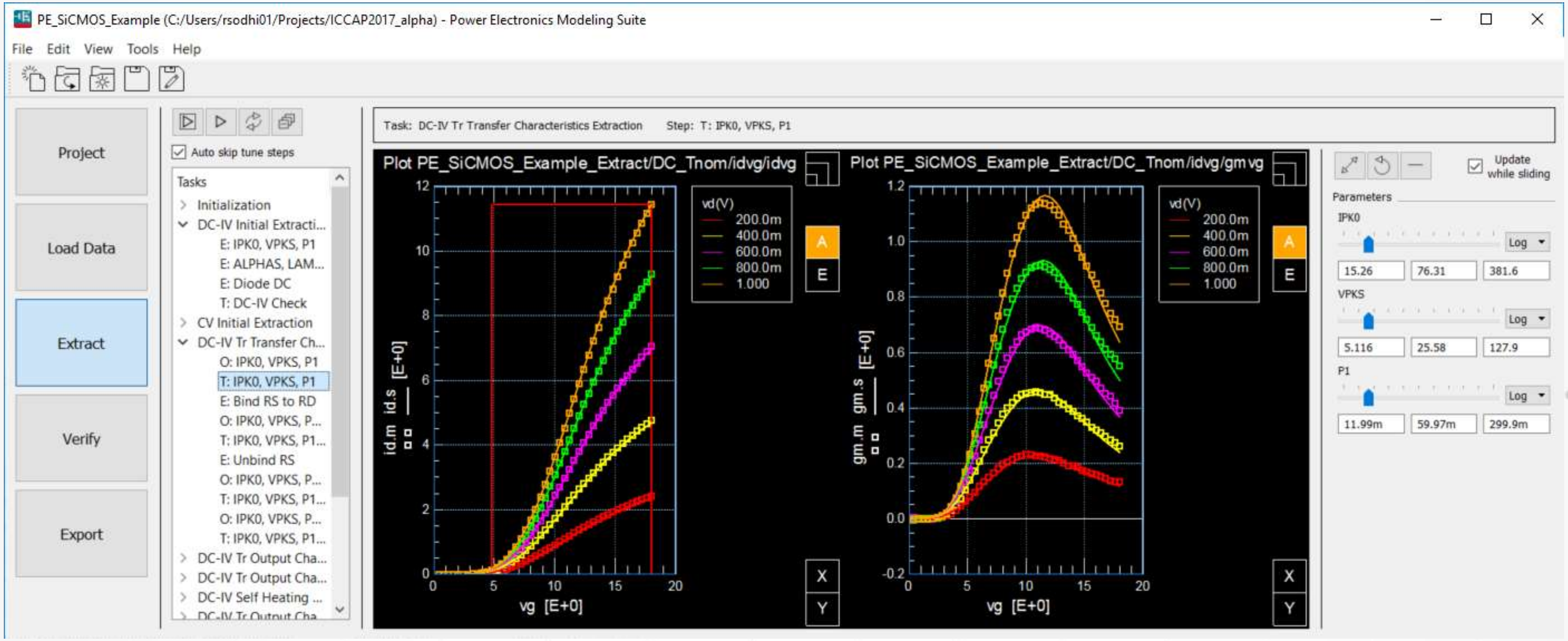
$$\tanh XX(i) = 1 + \tanh\left(A + B \times V_{gs} + C \times V_{ds}\right)$$

Added tanhXX to express a positive bias dependence on charge equation

- Modified popular Angelov GaN
  - To represent SiC or GaN behavior better
  - Independent of device physics parameters (e.g. Tox) → Everyone (e.g. circuit designer) can use it

Source: "Measurement Methodology for Accurate Modeling of SiC MOSFET Switching Behavior over Wide Voltage and Current Ranges", H. Sakairi, et. al., IEEE Trans on Power Electronics early access,

Power Electronics Model Generator



☑ Auto skip tune steps

Task: DC-IV Tr Transfer Characteristics Extraction Step: T: IPK0, VPKS, P1

☑ Update while sliding

Parameters

IPK0: 15.26 76.31 381.6

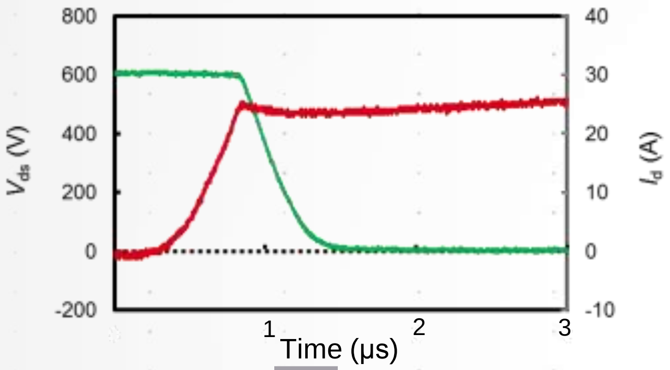
VPKS: 5.116 25.58 127.9

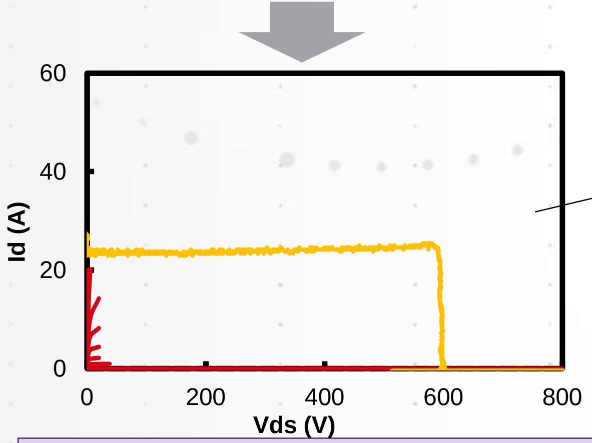
P1: 11.99m 59.97m 299.9m

- Powerful flow dynamically adapts to measured data and provides turns-key automated extraction of Power Electronics models

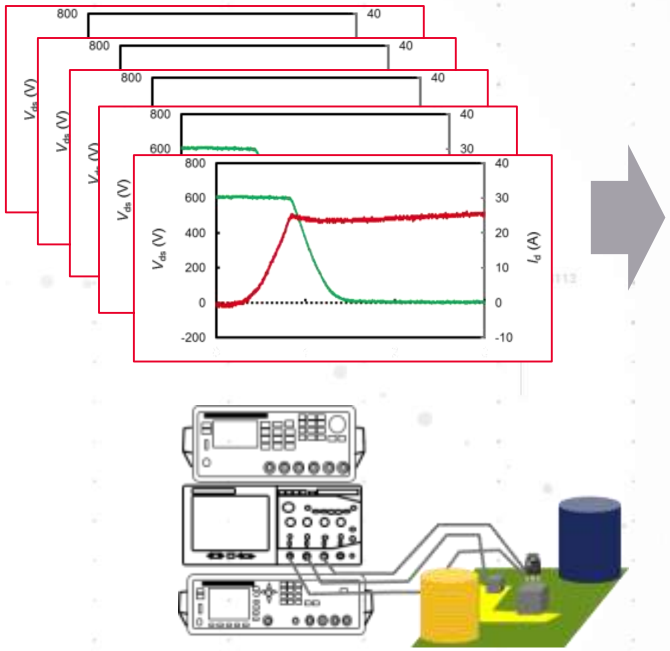
What are different? (2)

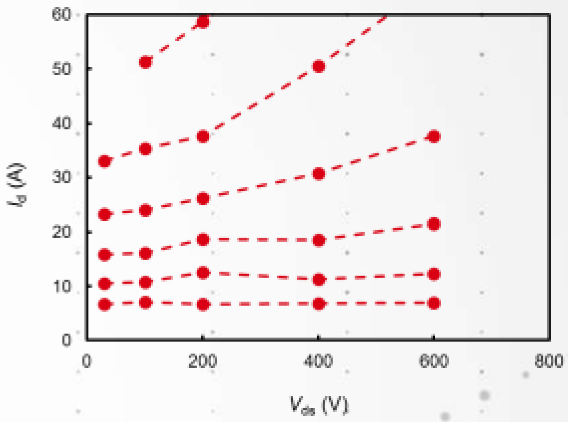
(A) Wide range IV using double pulse test





IV curve with conventional test equipment doesn’t cover switching trajectory





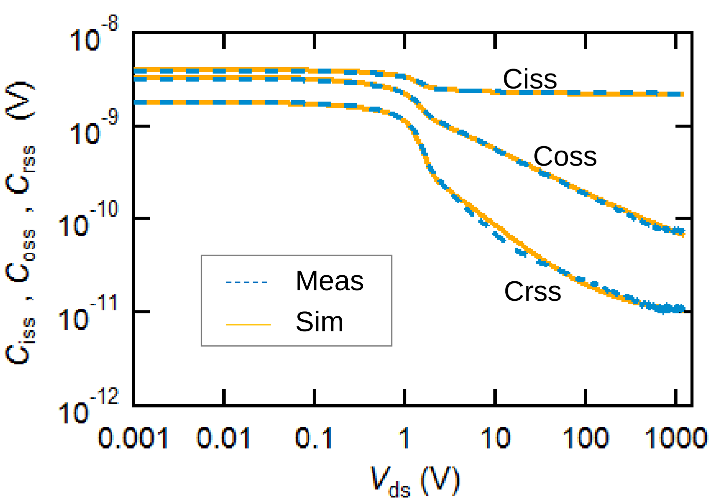
Wide range IV curve

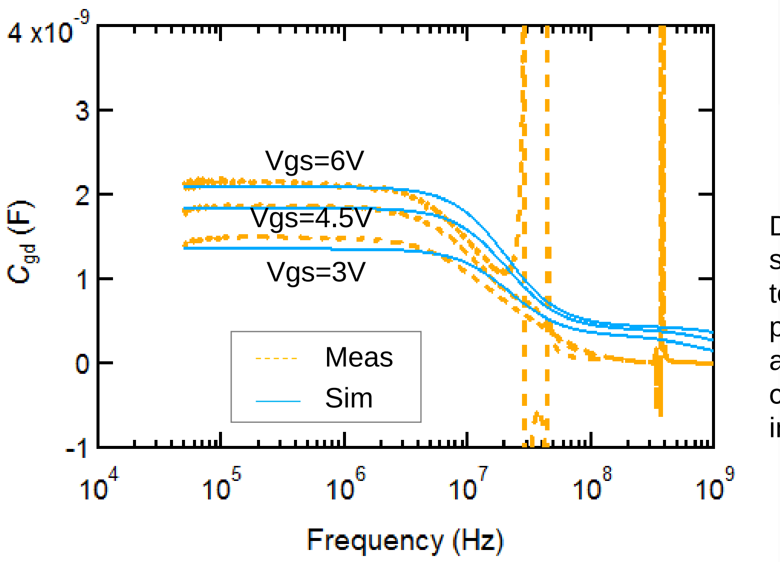
- Utilize double pulse test system to obtain wide enough IV curve to cover switching trajectory

Source: “Measurement Methodology for Accurate Modeling of SiC MOSFET Switching Behavior over Wide Voltage and Current Ranges”, H. Sakairi, et. al., IEEE Trans on Power Electronics early access,

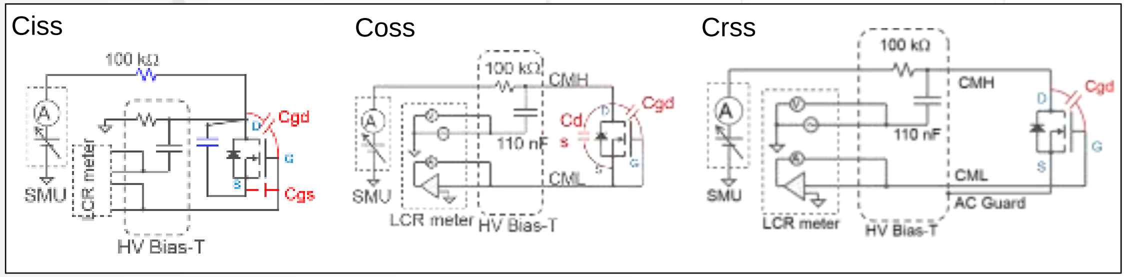
What are different? (3)

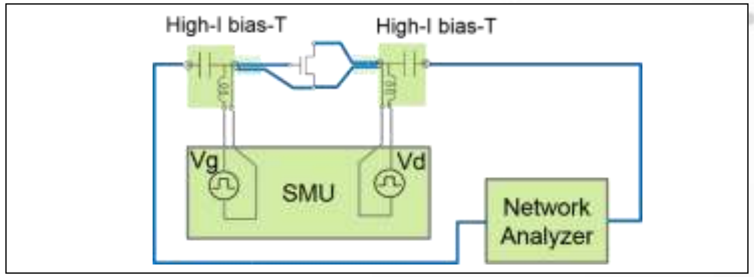
(B) Inclusion of CV (both off-state & on-state)





Discontinuous measurement points seen beyond 10MHz are considered to be caused by oscillation due to parasitic and stray inductance associated with measurement circuit. Therefore, simulation didn't include those points.



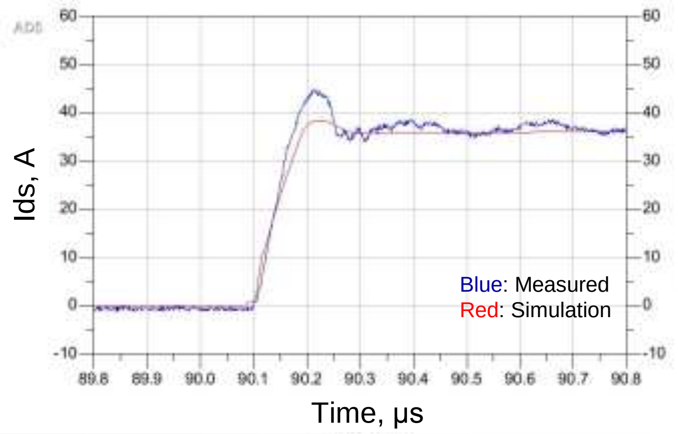


- Inclusion of non-linear characteristics is critical to represent device physical phenomena better

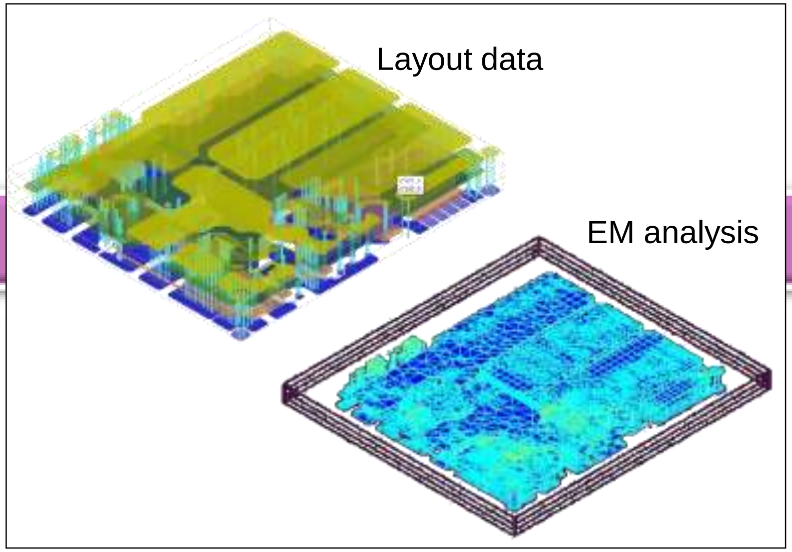
Source: "Measurement Methodology for Accurate Modeling of SiC MOSFET Switching Behavior over Wide Voltage and Current Ranges", H. Sakairi, et. al., IEEE Trans on Power Electronics early access,

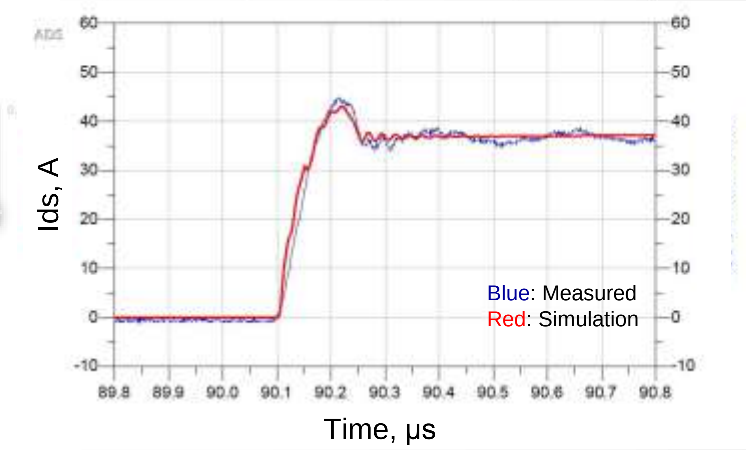
What are different? (4)

To use simulation software that performs not only time domain analysis but also incorporate electro-thermal and layout distribution effects



Improved device model without extensive EM simulation





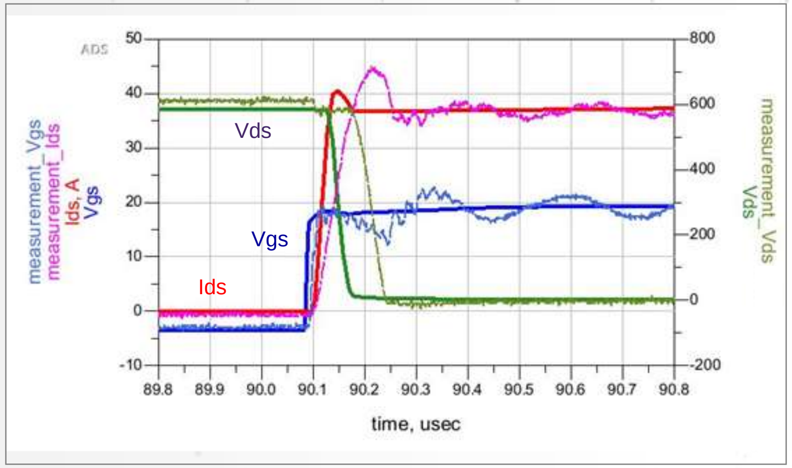
Improved device model with extensive EM simulation

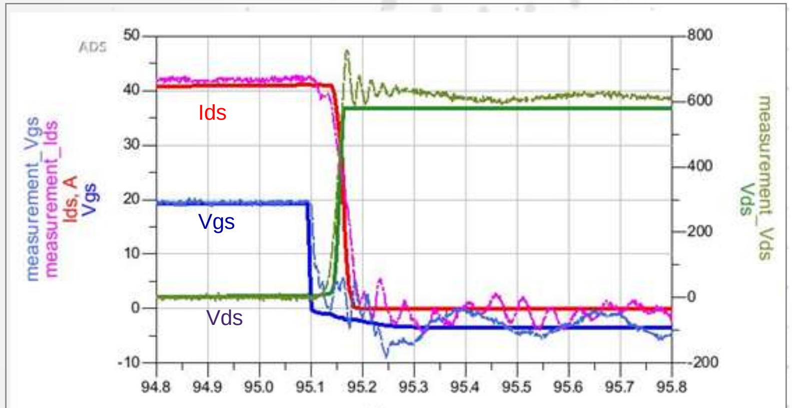
Electromagnetic simulation using board layout information as well as inclusion of s-parameters measured on DUT, the simulation of circuit operation becomes significantly better.

Source: “Measurement Methodology for Accurate Modeling of SiC MOSFET Switching Behavior over Wide Voltage and Current Ranges”, H. Sakairi, et. al., IEEE Trans on Power Electronics early access,

Circuit simulation based on the model and electromagnetic analysis

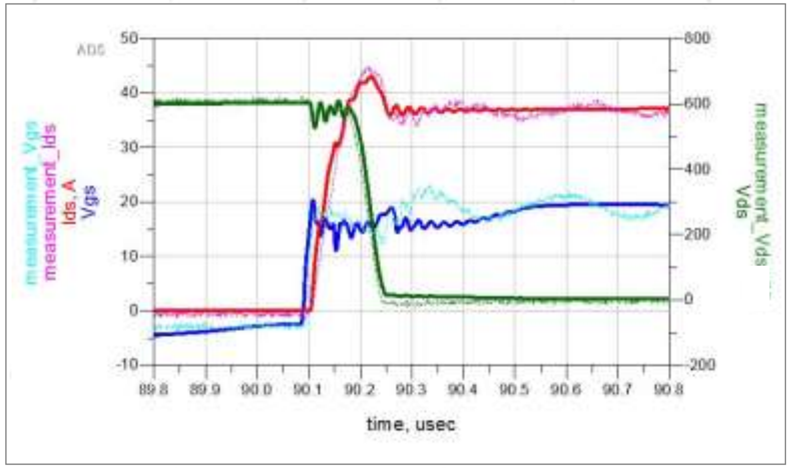
Conventional

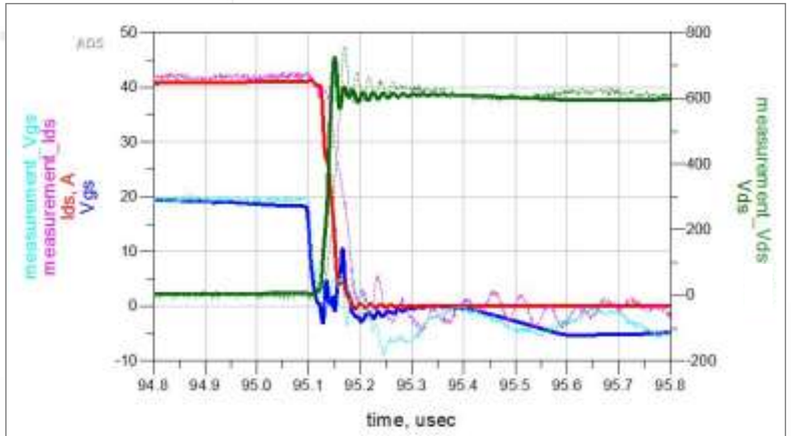


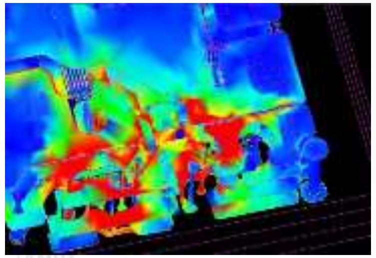


Solid line: simulation
Dashed line: measurement

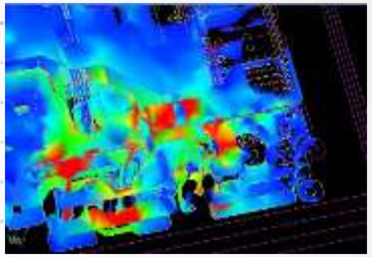
New method







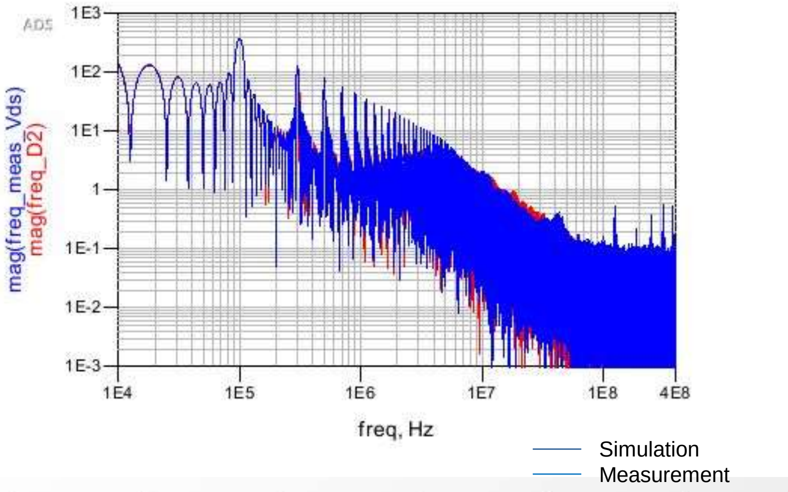
F=100kHz



F=900kHz

Frequency characteristics

Vds Power in mag : Sim and Meas

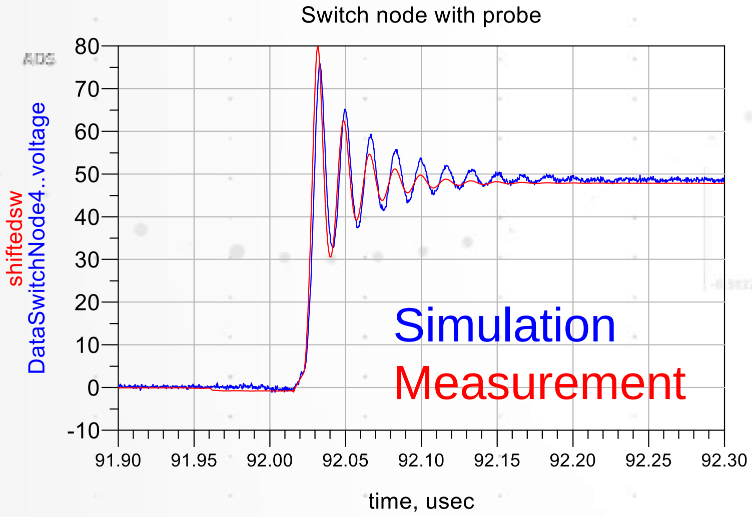


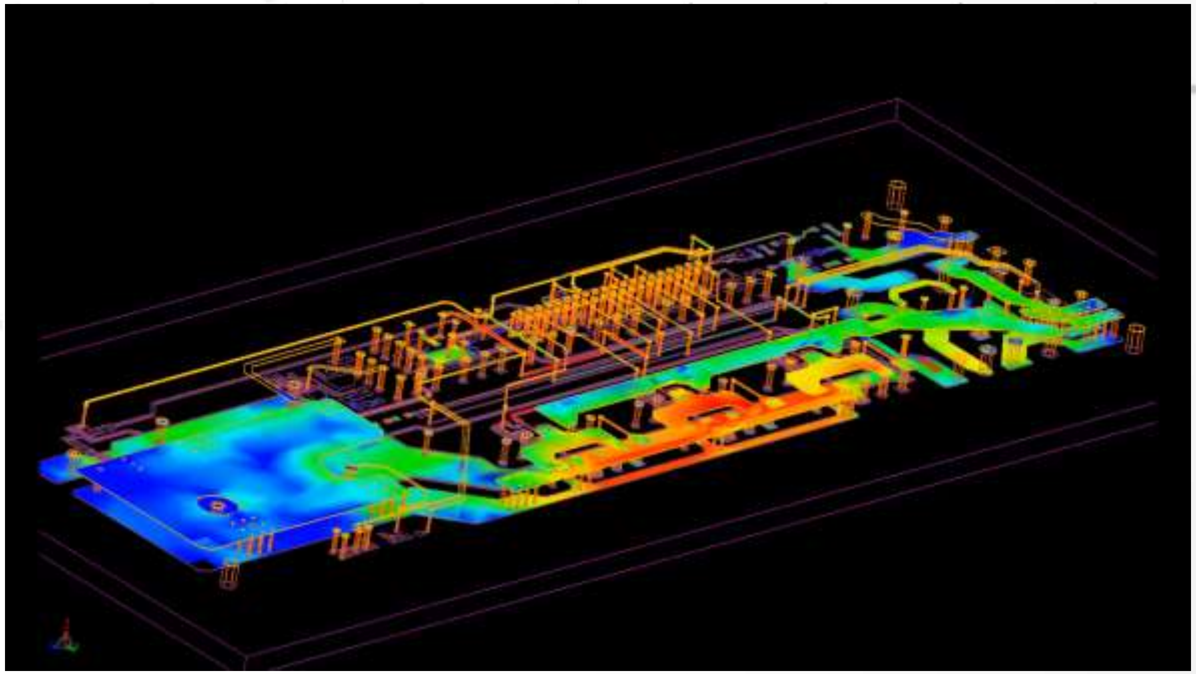
Source: “Measurement Methodology for Accurate Modeling of SiC MOSFET Switching Behavior over Wide Voltage and Current Ranges”, H. Sakairi, et. al., IEEE Trans on Power Electronics early access,

Results from EM-circuit Co-simulation

- EM-model informs the circuit simulation

- Circuit excitation informs the EM post-simulation visualization display





Insights Given From the Simulated Spectrum

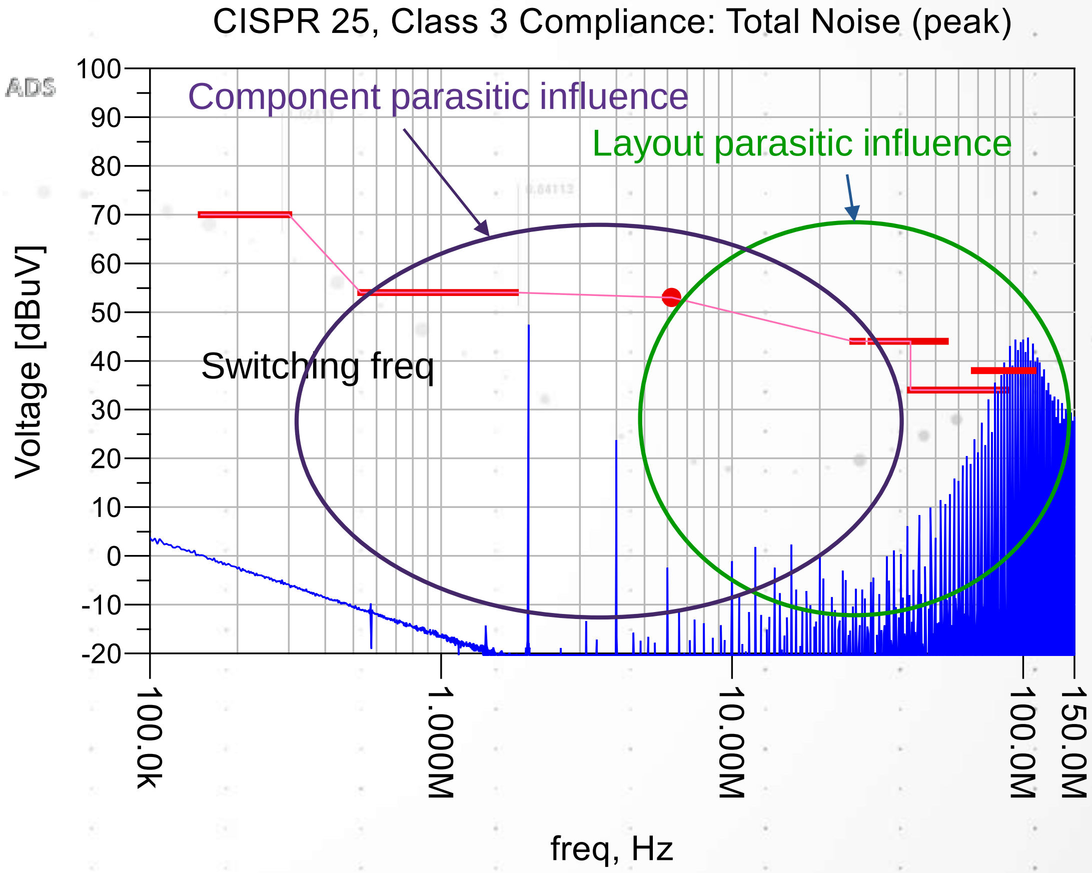
LAYOUT RELATED NOISE IS GREATER AT FM BAND

Underlying EMI mechanisms:

- Harmonically related components
- Non-harmonic related ringing
- Instabilities
- L di/dt mechanisms

Component and layout parasitics:

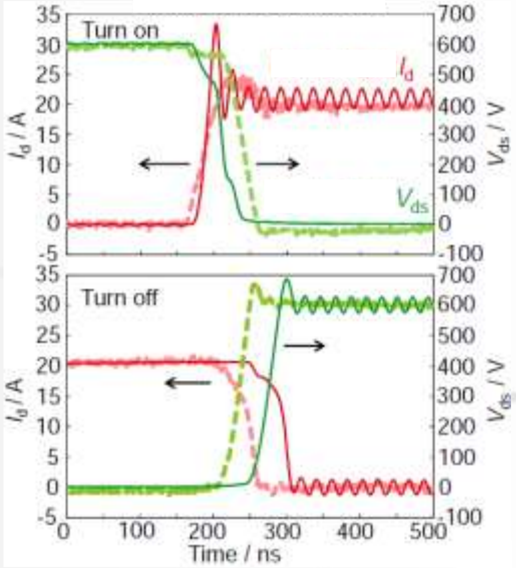
- Prevent EMI from being suppressed – they always need to be modeled
- May create noise in different frequency spectrums



Enabling technology

Simulation with a conventional model

Dotted: Measured
Solid: Simulation



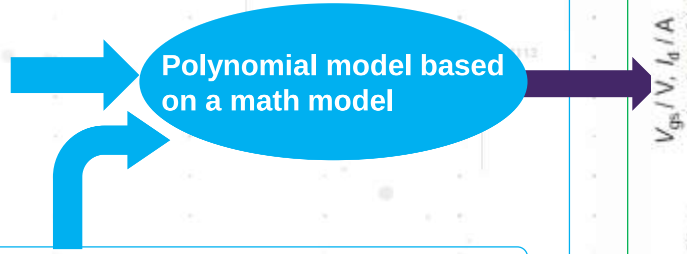
Waveforms don't match.
Exact waveform match is critical for noise calculation as waveform contains high frequency components

Apply Keysight mathematical model and key measurement data

Keysigh math basic current equation

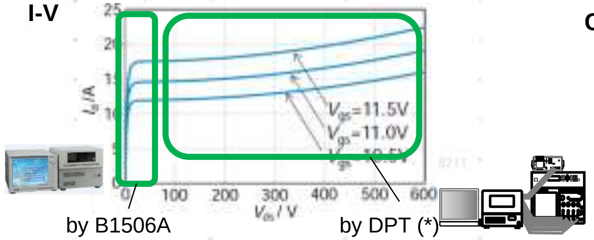
$$I_{ds} = I_{pk0} \times \left(1 + \tanh(\varphi)\right) \times \tanh(\alpha \times V_{ds}) \times (1 + \lambda \times V_{ds})$$

- Specially developed mathematical model uses tanh in current equation or capacitance equation
- Good convergence
- Easy to represent complex IV or CV
- Less number of parameters (< 100)
- Generic and applicable regardless of material or structure



Polynomial model based on a math model

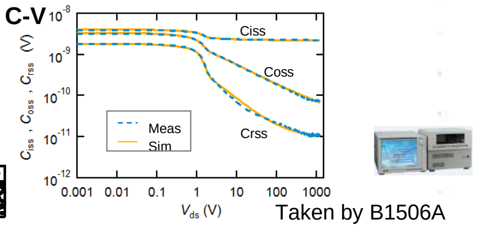
I-V



by B1506A

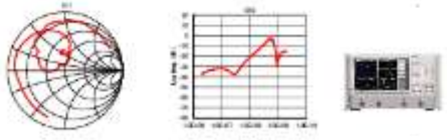
by DPT (*)

C-V

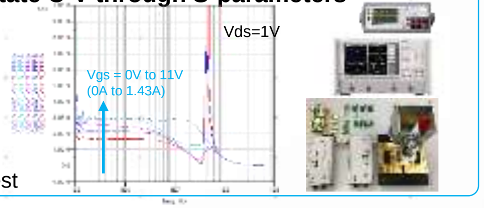


Taken by B1506A

S-parameters for circuit parasitic



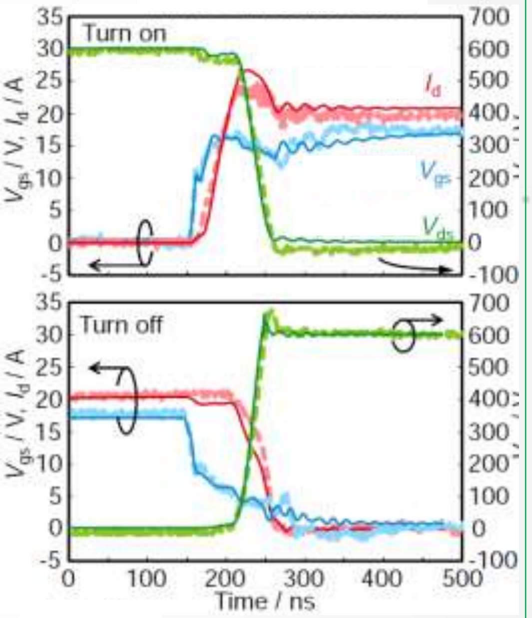
On-state C-V through S-parameters



* DPT = Double pulse test

Simulation with the Keysight math model

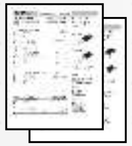
Dotted: Measured
Solid: Simulation



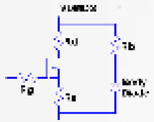
Excellent matching between simulation and measurement

Source: "Measurement Methodology for Accurate Modeling of SiC MOSFET Switching Behavior over Wide Voltage and Current Ranges", H. Sakairi, et. al., IEEE Trans on Power Electronics early access,

Before & After Our Solution

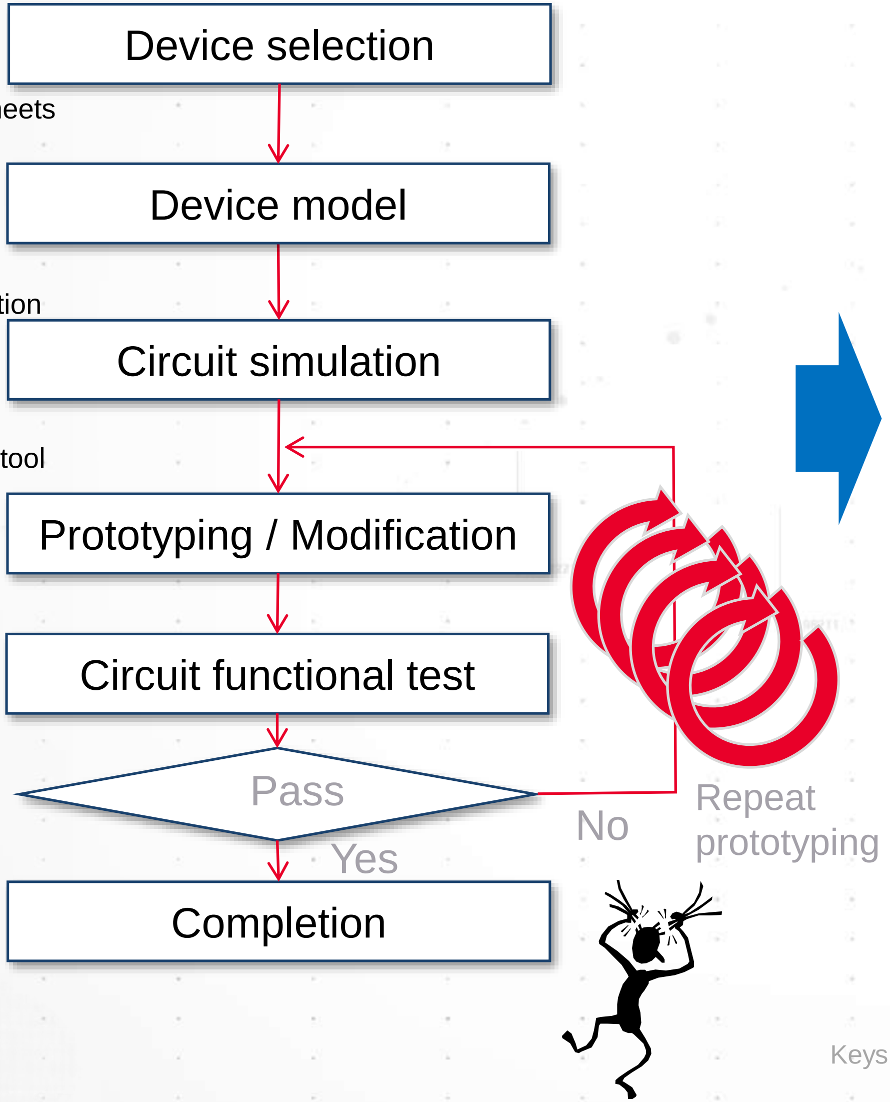


Unreliable vendor datasheets



poor device model to produce trustable simulation

Cheap & inaccurate SIM tool



Device selection

Device model

Circuit simulation

Prototyping / Modification

Circuit functional test

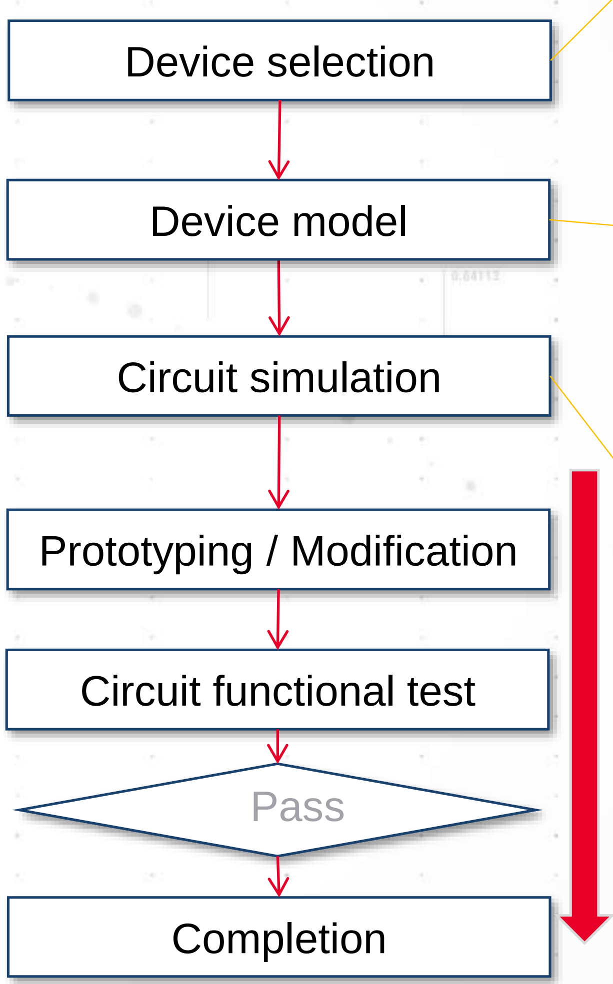
Pass

No

Yes

Repeat prototyping

Completion



Device selection

Device model

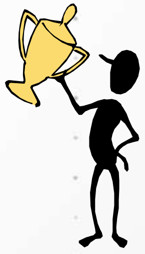
Circuit simulation

Prototyping / Modification

Circuit functional test

Pass

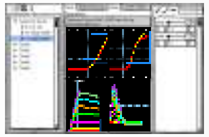
Completion



Keysight instruments

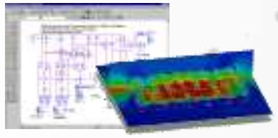
Sure selection & accurate data extraction for model creation

Keysight PE model generator



Measurement driven polynomial model based on a math model

Keysight ADS PE Bundle

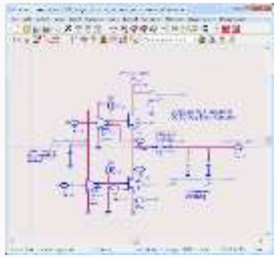


Reliable time domain & EM simulation based on reliable model

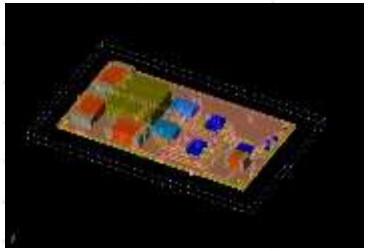
Keysight Integrated Power Electronics Solution

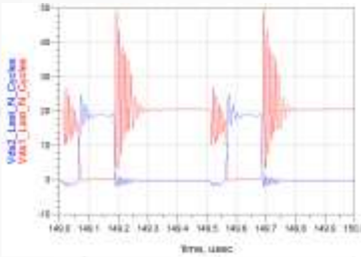
ADVANCED DESIGN SYSTEM (ADS)

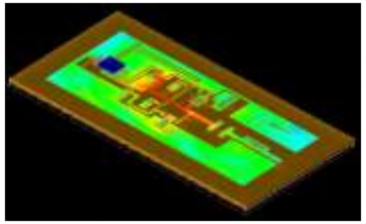
W2240 Power Electronics Bundle

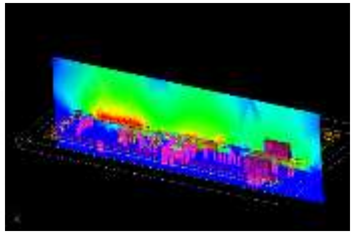

Schematic


Layout

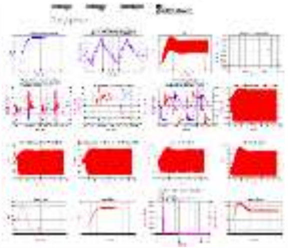

3D viewer


Transient/convolution


Momentum

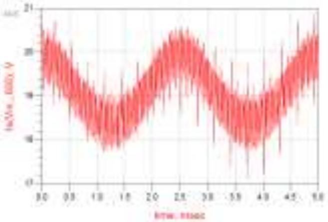

FEM

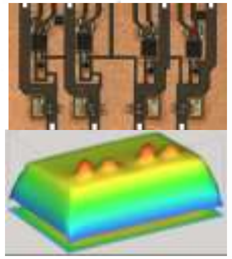
Power Electronics Library


Data display


Verilog-A

Product Options


W2300 Harmonic Balance Simulator


W2349 Electro-Thermal Simulator

Keysight Solutions for Power Electronics

KEY CHALLENGES OUR CUSTOMERS ARE FACING TODAY

PE Design Challenges

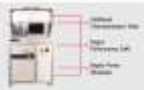
- Mitigate noise on Switching (← Reliability, EMI Standards)
  Surge Voltage, di/dt, Conductive noise
- Thermal design (← Reliability)
  Thermal distribution on PCB (Air flow is partially supported)
- Improve power efficiency (← Efficiency)
  Switching Losses, Conductive losses

Device Modeling

Device Parameter Measurement

IATF Compliant Cal

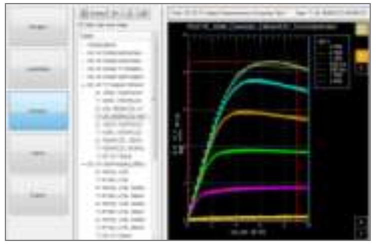
B1506A Curve Tracer / Power Device Analyzer
I-V, C-V



Double Pulse Test PD1500A NEW
High power I-V

E5080A ENA + Fixture NEW
Zero-bias S-param, On-state C-V

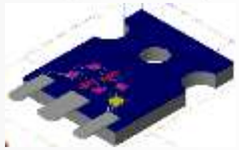
Parameter Extraction

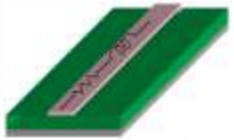


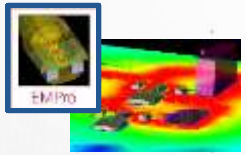
1. **Power Electronics Model Generator** NEW
   Simple and quick fitting
2. **IC-CAP based Power MOS/SiC/GaN/IGBT Modeling Opt.** NEW
   For professional, high accurate modeling
3. **Keysight Modeling Service**

Parasitic Effect Consideration

Packaged/Passive modeling





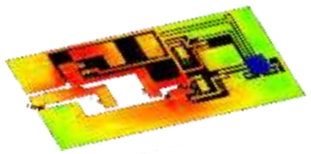


ADS Full 3D EM/EMPro
EM based simulation

IATF Compliant Cal

Network Analyzer
Verification of devices

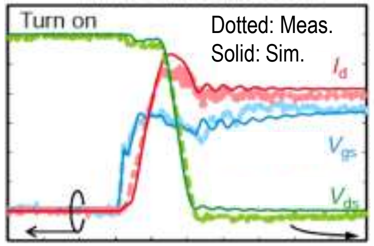
Board Pattern Modeling



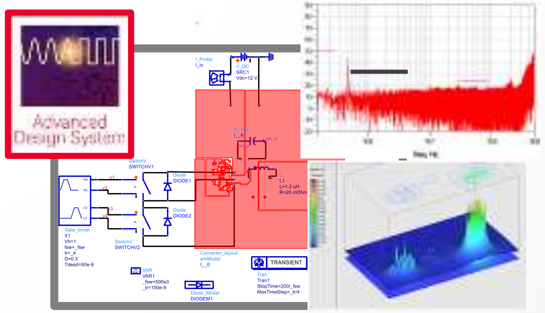
ADS 3D-Planar EM Sim.
Allows the most accurate design

Circuit Development

Simulation Design

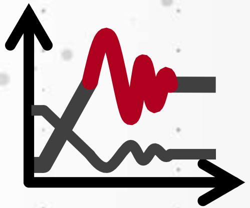


Source: IEICE the 29th Workshop on Circuits and Systems



ADS PE Bundle
De-fact standard circuit simulator considering

Real Measurement



IATF Compliant Cal

Oscilloscope
Waveform analysis and debugging

KEYSIGHT TECHNOLOGIES

KEYSIGHT
WORLD 2019