KEYSIGHT WORLD 2019

400G: Looking Forward to 800G and Terabit Speeds

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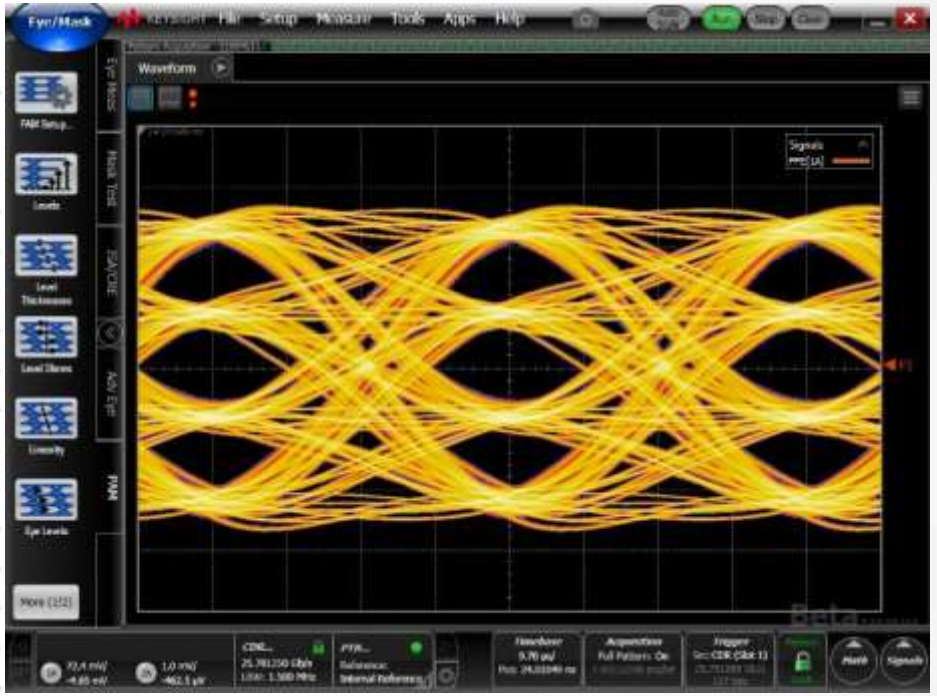
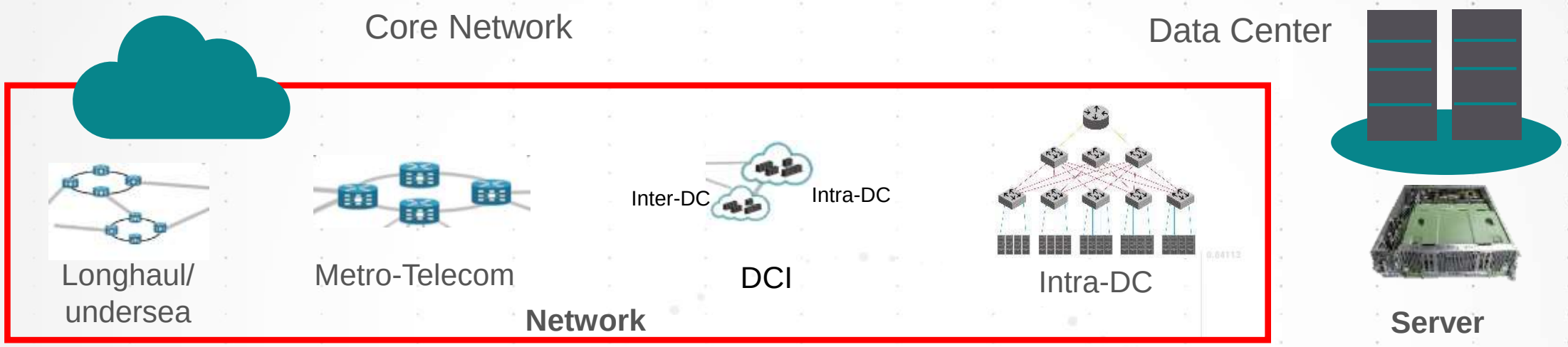
Agenda

- Introduction
- PAM4 Simulation
- 400G -> 800G Measurements
  - Direct Detect Output (Transmitter) Test
  - Direct Detect Input (Receiver) Test
  - Coherent Optical Test
  - Layer 2-3 Analysis
- Summary



Wireline Internet Infrastructure

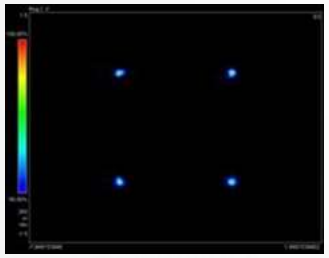
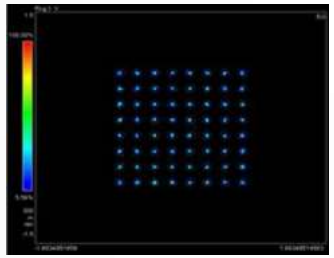
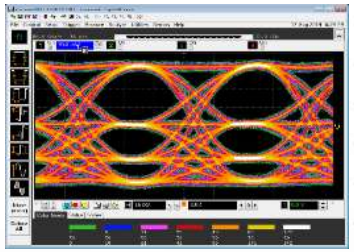
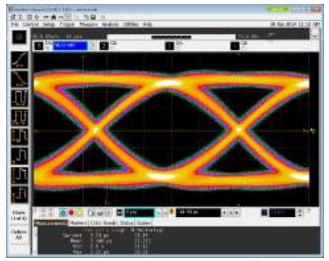


Longhaul/ undersea	Metro-Telecom	DCI	Intra-DC	Server
100 km – 39,000 km 60 mi – 24,000 mi	10 km – 100 km 6 mi – 60 mi	10 km – 40 km 6 mi – 25 mi	20 m – 10 km 22 yd – 6 mi	1 mm – 3 m .04 in – 10 ft

Coherent
How low can you go?

?

NRZ / PAM4
How far can you go?

Why Does the Industry Need PAM4?

ENABLES HIGHER DATA THROUGHPUT

- NRZ > 28 Gb/s limits trace length or increases cost
- PAM4 yields 2 bits / symbol
  - ✓ Effectively halves the channel BW needs
- Allows designers to develop products to fit the cost structure of available channel technologies.

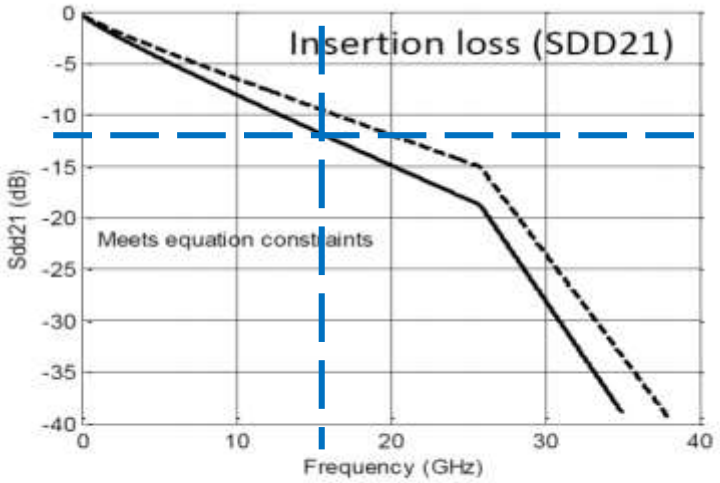
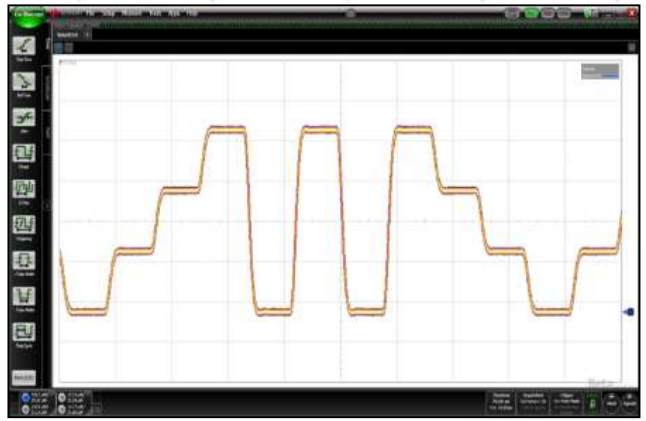
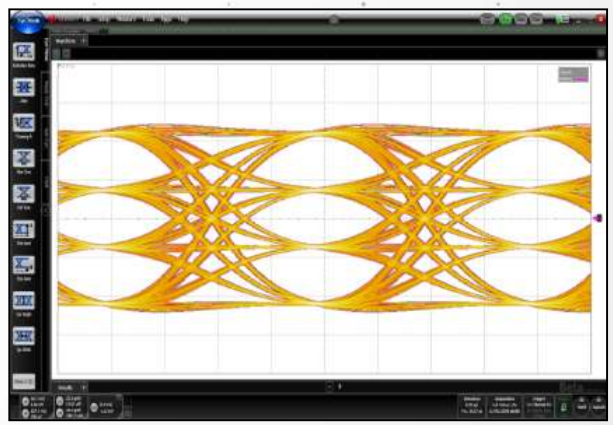


Figure 5: CEI-56G VSR NRZ channel

- PAM4: Pulse Amplitude Modulation 4-level
- 2 bits of information in every symbol
  - ✓ ~ 2x throughput for the same baud rate
  - ✓ 26.56 Gbaud PAM4 = 53.125 Gb/s
- Lower SNR, more susceptible to noise
- More complex Tx/Rx design, higher cost





State of the '400G Class' Standards

CURRENT GENERATION - 50G LANE RATE

✓ • OIF-CEI-56G 5 reaches PAM4 up to 29 Gbaud, NRZ up to 58 Gb/s	Released
✓ • IEEE 802.3bs 200/400G (Ethernet) Medium reach SMF + C2C,C2M, PAM4 @ 53.1 & 26.6 Gbaud	Released
✓ • IEEE 802.3cd: 50/100/200G (Ethernet) Short reach MMF. + C2C,C2M, backplanes & cables, PAM4 @26.6 Gbaud	Released
✓ • 64G Fibre Channel 100m – 2 km reaches in MMF & SMF, PAM4 @ 28.9 Gbaud	Complete, pending publication
✓ • COBO version 1.0 (Optical PHY from 802.3bs, Elec. from OIF-CEI-56G-VSR)	Released
• IEEE 802.3cm 400G Short reach in MMF, PAM4 @ 26.6 Gbaud	Under development
• IEEE 802.3cn 50/100/200/400G 10 km SMF, PAM4	Under development
• OIF 400ZR 80 km SMF, DP-16QAM @ 60 Gbaud, coherent	Under development
• IEEE 802.3ct 100/400GBaseZR 80 km SMF, DP-16QAM, coherent, (based on OIF 400ZR)	Under development

Next-Generation ‘800G Class’ Standards

112G LANE RATES

• OIF CEI-112G 5 reaches PAM4, CNRZ-5	Project starts for 5 reaches, C2M at 7th draft
• IEEE 802.3ck C2M & C2C for 2nd wave 400GbE & 800G	First baseline draft for C2M May2019 (based on OIF CEI-112G-VSR, MR, and LR)
• Fibre Channel PI-8 128GFC Moving closer to Ethernet baud rate	Project Start

Is 800G Really Starting Yet?

- First equipment using 400G is close to deployment
- Few remaining initial wave of ‘400G class’ standards finishing up
- No 802.3 official study groups started for first 800G optical links yet
- Electrical chip-to-module, chip-to-chip, and backplane interface projects have started supporting >112 Gb/s per lane

Thoughts / Assumptions 800G Enabling Technologies

- Optical – 56 Gbaud PAM4 – Proven in 400GBASE-DR4 (part of 802.3bs)
- Electrical – mostly 56 Gbaud PAM4

- Most (but not all) detectors will digitize with DSP
- Optical and electrical links continue to rely on FEC to restore error free link
- FEC will pass through and not processed in module

- Will there be a 224G C2M AUI?
  - Not without higher bit/symbol modulation. Some multi-wire modulations are being studied.

400G Solution Overview

END-TO-END SOLUTIONS FROM KEYSIGHT

M8040A BERT

M8194A AWG

Receiver Test

N1000A DCA-X / N1092A DCA-M
Sampling Scope

UXR Real-time Scope

Transmitter Test

ARESONE-400GE

L2/L3 400GE Test

400G Design Cycle

PLTS + M980Xa VNA

Channel/ Interconnect

Modeling / Link Simulation

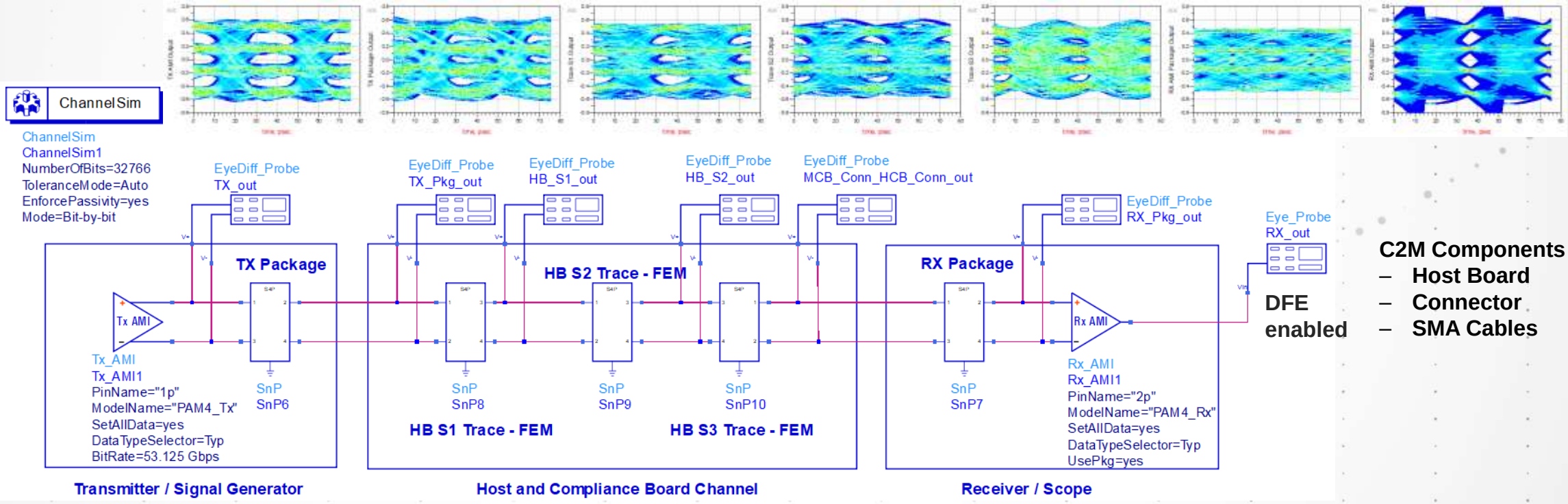
ADS, FlexDCA link

PAM4 Simulation

PAM4 Channel Simulation with AMI Model

EXAMPLE: 400G CHIP-TO-CHIP (C2C) TEST BENCH SETUP

- Keysight ADS SW provides comprehensive PAM4 Channel Simulation Analysis using vendor IBIS-AMI models
- Test Setup: TP0 to TP5 (ball-to-ball)



C2M Components
- **Host Board**
- **Connector**
- **SMA Cables**

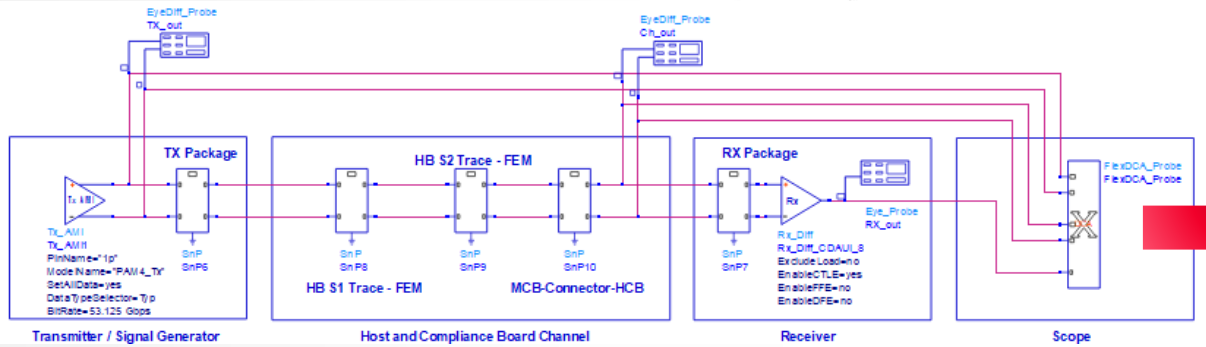
http://www.eda.org/ibis/

IBIS (IO Buffer Info Specification)
AMI (Algorithmic Modeling Interface)

Correlate PAM4 Simulations with Measurement

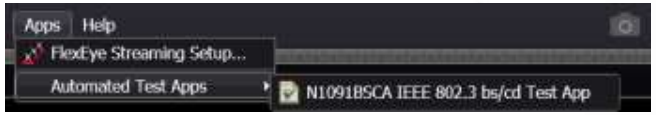
ADS 2019 TO FLEXDCA "CONNECTED FLOW"

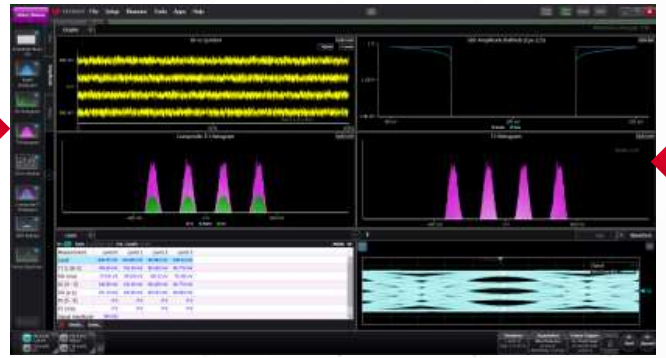
- Connects simulation and measurement domains seamlessly: **"Design to Test"**
- Uses the **same measurement algorithm** and methodology on both simulated and measured waveforms
- Expands ADS PAM4 measurement capabilities to include **Jitter analysis and TDECQ**
- Runs **compliance apps** on simulated and measured waveforms



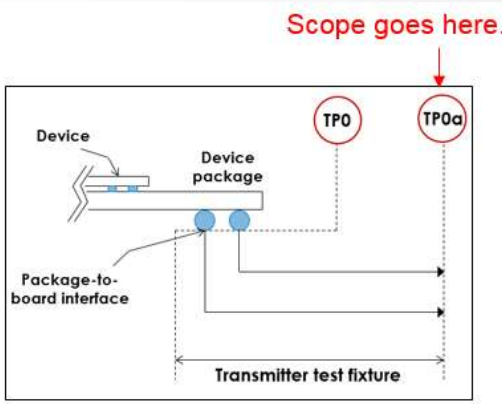
ADS
Simulation Domain

Compliance Apps

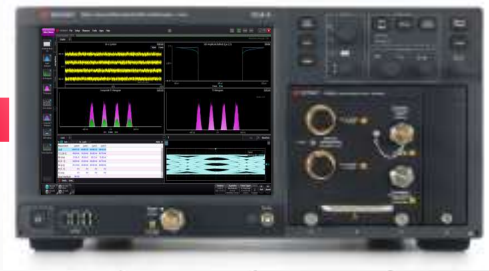




FlexDCA – Eye/Jitter Analysis



Transmitter compliance measured at TP0a

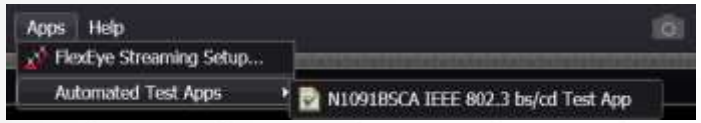


DCA-X Oscilloscope
Measurement Domain

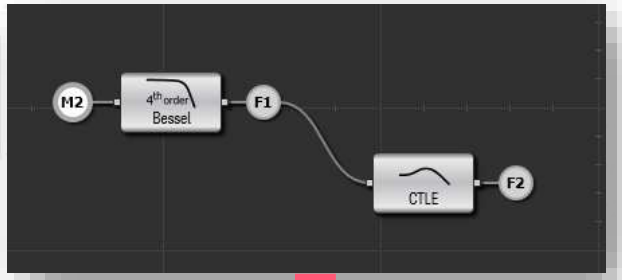
PAM4 Analysis using ADS 2019 and FlexDCA

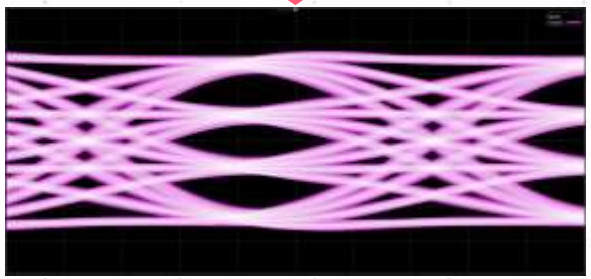
PAM4, JITTER, COMPLIANCE APPS

- ADS starts FlexDCA automatically
- Unlock all built-in comprehensive PAM4 analysis in FlexDCA
  - Eye contour
  - TDECQ (Transmitter Dispersion Eye Closure Quaternary)
  - Outer OMA
  - Linearity
  - Noise Margin
  - Partial SER
  - Partial TDECQ
  - Levels, Level Skews
  - Eye Skews, Height, and Width..
- Jitter Analysis
- Run Compliance Apps

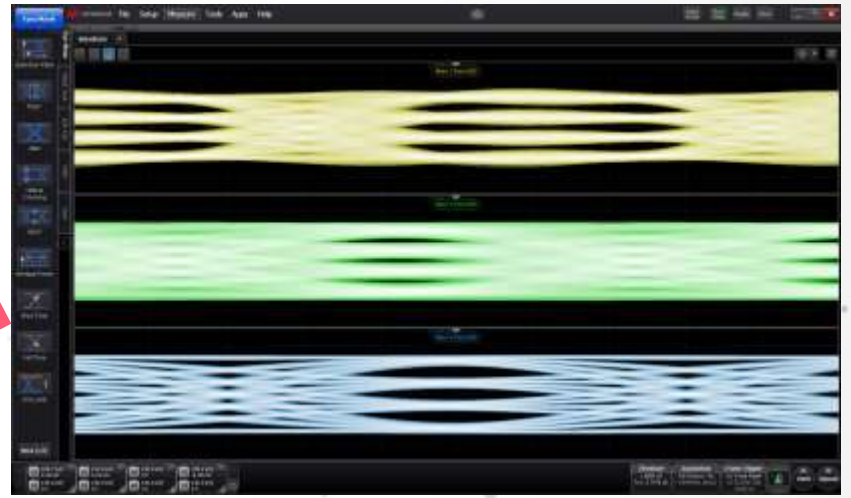


Math and DSP in FlexDCA





ADS Waveforms -> FlexDCA

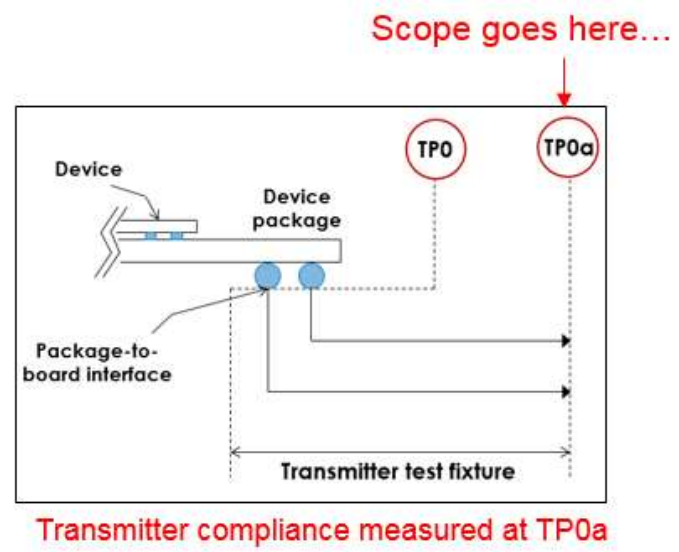


Jitter Analysis

Direct Detect Output (Transmitter) Test

Where Do the Tx Parameters Get Tested?

IEEE 802.3bs Electrical Tx Test Points



Chip-to-Chip (C2C) at TP0a (custom fixture)

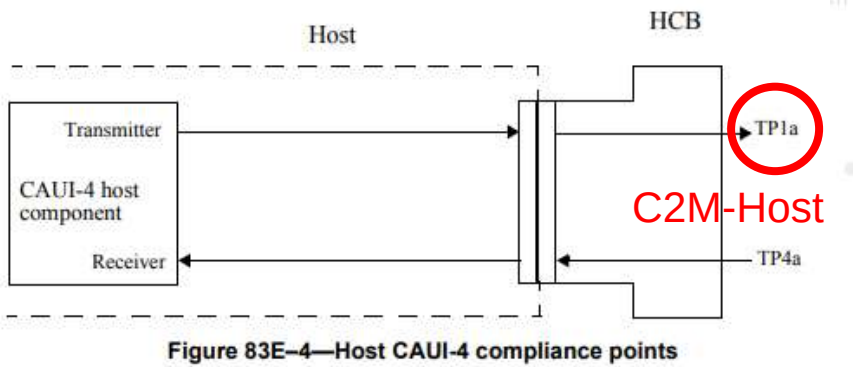


Figure 83E–4—Host CAUI-4 compliance points

Chip-To-Module (C2M) at TP1a (use compliant fixture)

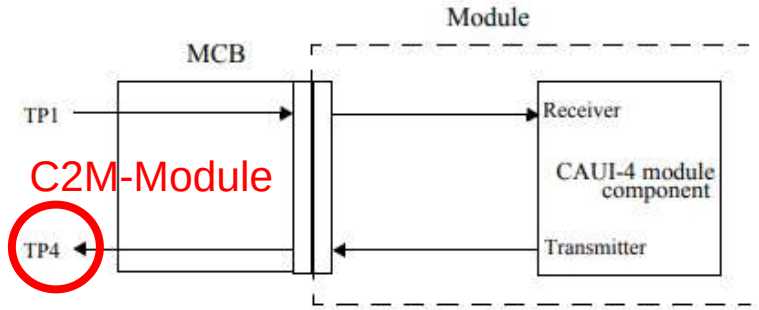


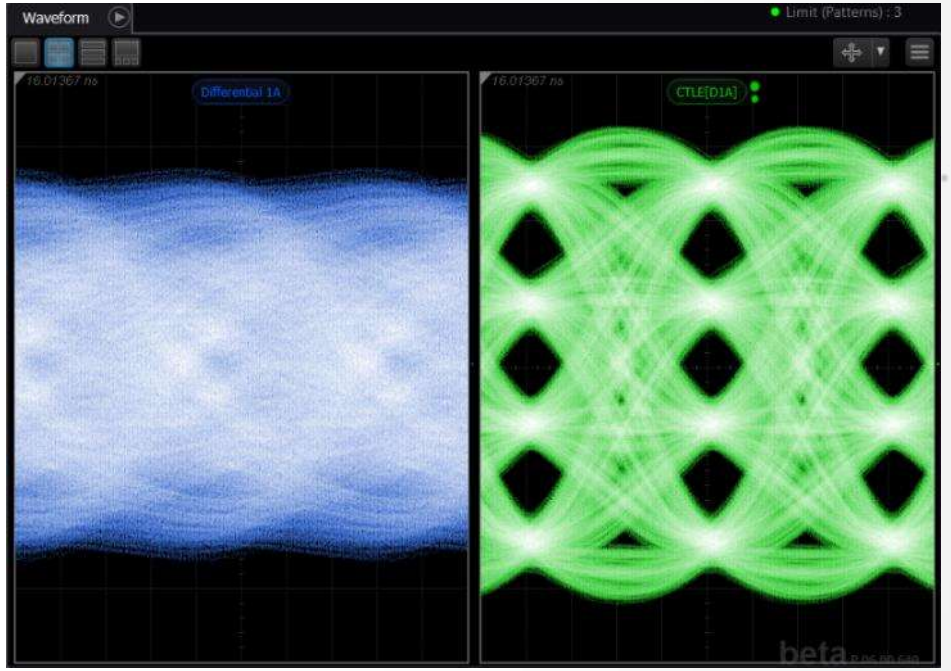
Figure 83E–5—Module CAUI-4 compliance points

Chip-to-Module Module Output (C2M) at TP4 (use compliant fixture)

Measurement Challenges for PAM4 Test

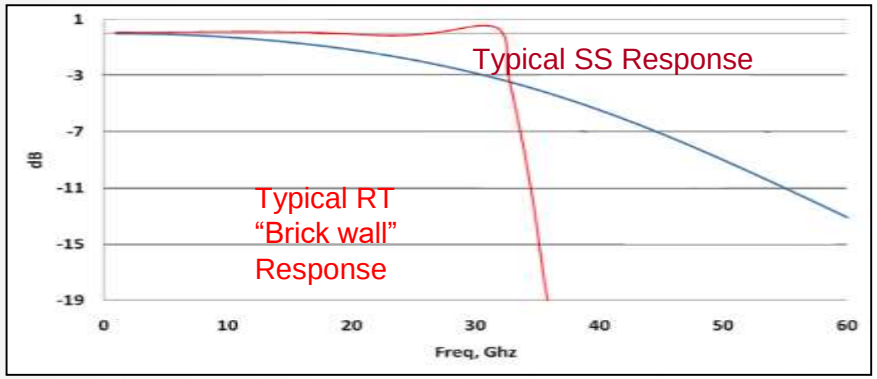
NEW ANALYSIS METHODOLOGY REQUIRED TO ANALYZE DEGRADED SIGNALS

- **Baud rates continue to increase (from 26 to 53 Gbaud)**
  - Standards (IEEE 802.3bs/cd, CEI 4.0,...) require:
    - ✓ higher bandwidth test equipment
    - ✓„ideal“ 4th Order Bessel-Thomson reference receiver response
    - ✓equalization to open signals for analysis
- **Degraded PAM4 Eyes**
  - Requires low noise reference receivers and advanced clock recovery
- **Complex New Measurements**
  - Requires advanced analysis tools



Compliant Frequency Response (Reference Receiver)

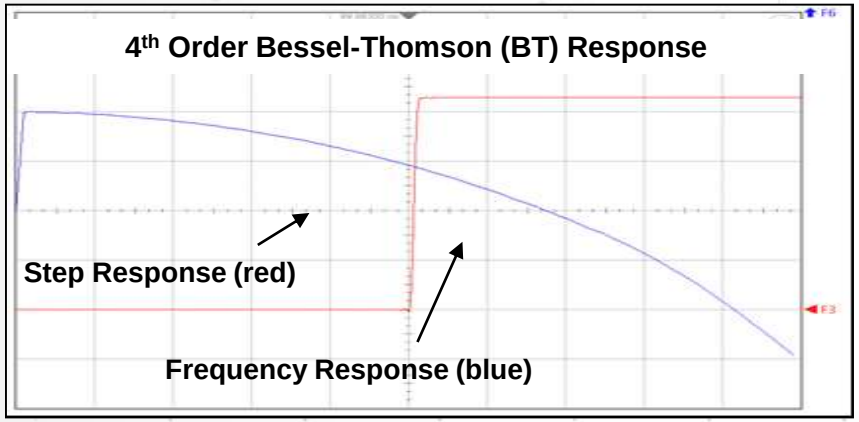
Receiver Frequency Response:



Scopes have different frequency responses:

- Will result in different eye/waveform shapes and amplitudes –> different measurement results
- To achieve 33/40 GHz 4th Order BT response on a RT scope, must start with > 60 GHz "brick wall" response

To provide more measurement consistency, most standards now specify BW and shape.



Examples (26 Gbaud PAM4; 53 Gb/s):

- **IEEE 802.3bs™/D3.5 (Ethernet)**

Clause 120D.3.1 200GAUI-4 or 400GAUI-8 transmitter characteristics:
"A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified."

- **CEI-56G-VSR-PAM4**

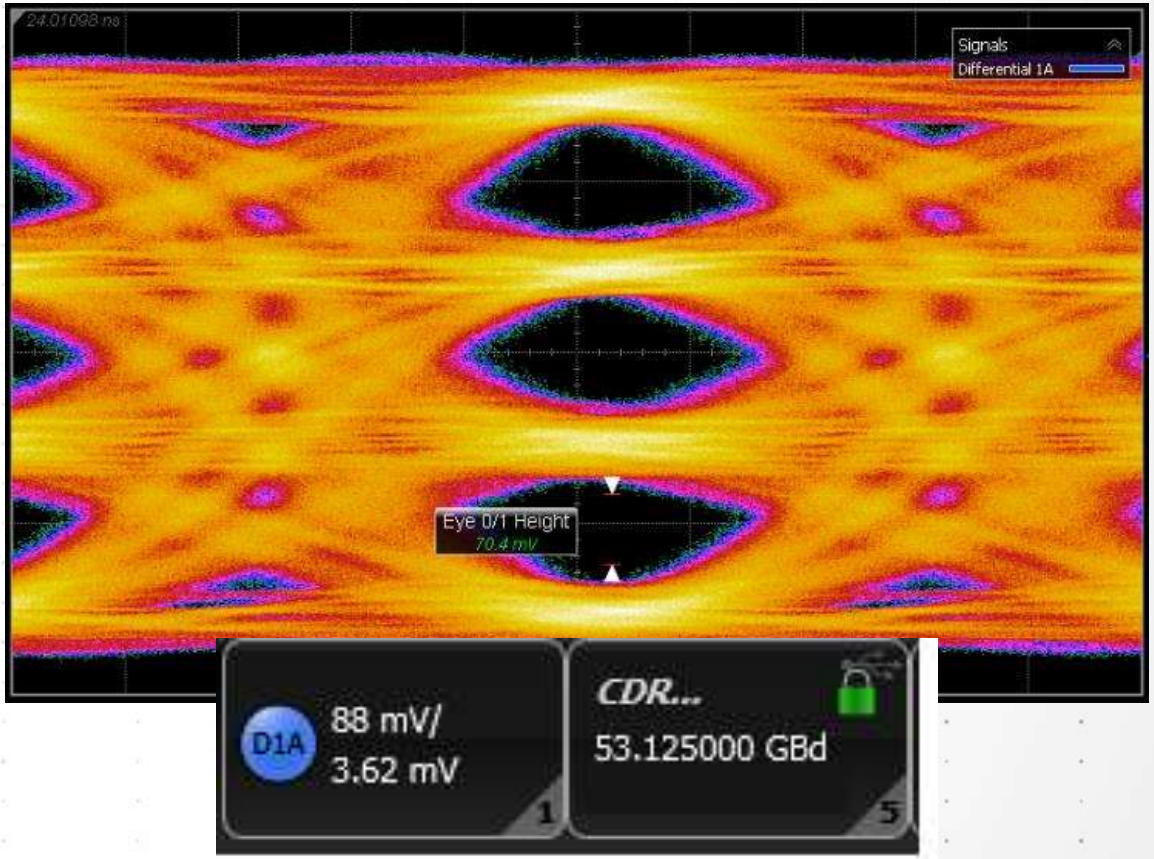
Section 16.3.4 Output Differential Voltage, pk-pk
"The waveform is observed through a fourth-order Bessel-Thomson response with a 3-dB bandwidth of 40 GHz using a QPRBS13-CEI pattern."

Bandwidth for “112G” (56 GBd)

PROPOSED 43 GHZ BESSEL

- 43 GHz Bessel response is deemed to be representative of “112G” transmitters (chip -> package -> fixture)

- Will this be sufficient BW for Tx characterization? Will 43 GHz BW penalize (reduce EH/EH margins) designs with better SI performance?



Clock Recovery for PAM4 Designs

Clock recovery (CR)

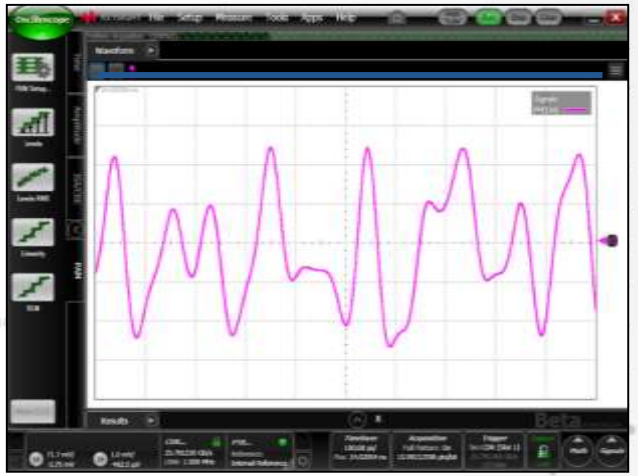
- Recovers a clock for the Rx to use in real systems
- Scopes need to emulate CR used in real Rx
  (track out low-frequency jitter, trigger the scope)

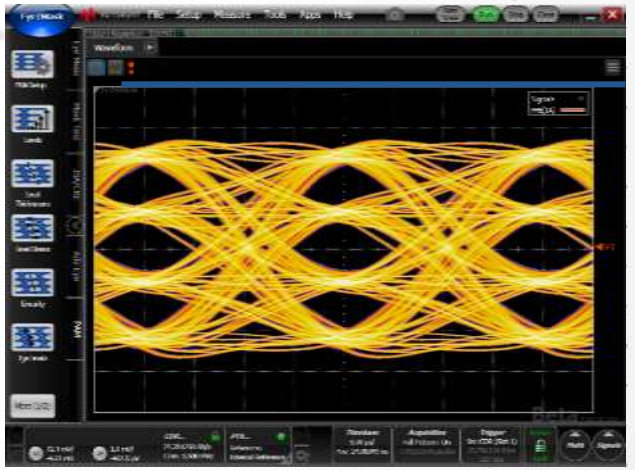
PAM4 adds complexity

- Transitions no longer only at 0V diff
- CR Loop BW reduced from 10 MHz to ~ 4 MHz
  (IEEE 802.3bs/cd and CEI-56G-PAM4, same for 112G standards)

Instrument clock recovery

- Real-time oscilloscopes use software CR
- Equivalent-time oscilloscopes (aka Sampling scopes) use hardware CR
- CR needs to be able to lock onto “closed eyes”

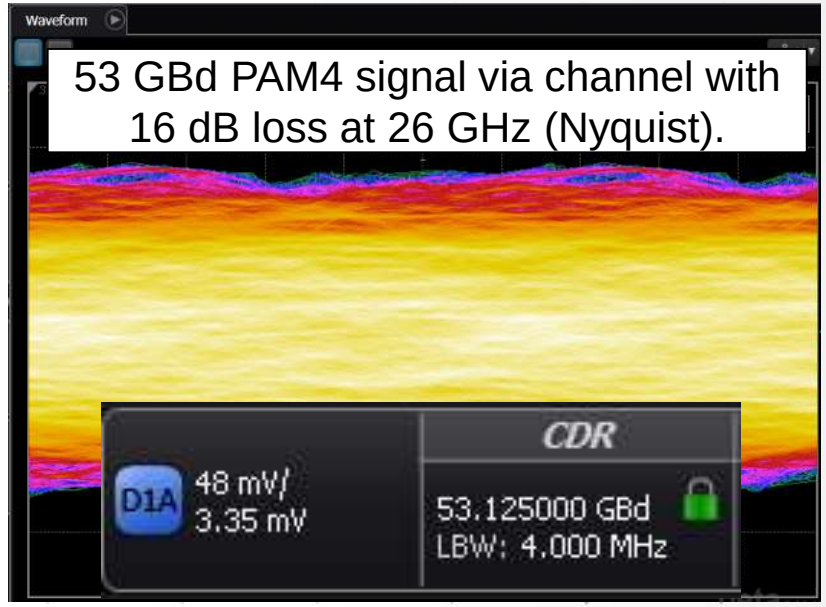




Analyzing Degraded PAM4 Signals at 53 Gbaud (112G)

HIGHER CHANNEL LOSS, XTALK, AND REFLECTIONS AT 53 GBAUD (106 GB/S)

C2M Channel Insertion Loss (IL): Up to 16dB at 26.56 GHz (proposed). Whole link insertion loss can be more than 20dB.



Step 1: Scope must obtain CR lock (SW or HW) in order to analyze/equalize signals

- Ensure the CR in your instrument can lock onto severely closed eyes

Step 2: Equalize the signal and analyze

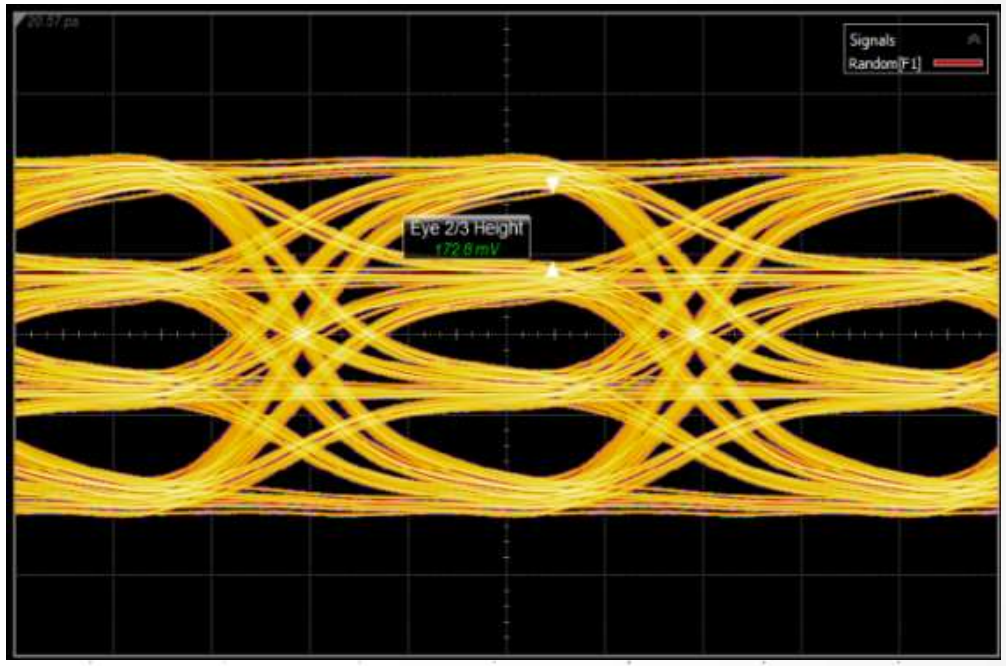
- **"56G" Today:** only uses CTLE (up to 9 dB)

- **"112G" Future:** will likely require a combination of CTLE, FFE (5 tap?, 12 tap?), and/or DFE

Which Tx parameters Get Tested?

KEY PAM4 MEASUREMENTS FOR ELECTRICAL TRANSMITTERS

- **Eye Width (EW), Eye Height (EH)**
- **Eye Symmetry Mask Width (ESMW)**
- **Output waveform**
  - Level Separation Mismatch Ratio
- **Signal-to-noise-and-distortion ratio** (SNDR)
- **Output jitter**
  - J_{RMS}
  - J3u, J4u
  - Even-Odd Jitter (EOJ)



While these parameters may sound familiar to you, they are measured very differently compared to legacy NRZ designs

Output Jitter: Characterize 12-Edges of a PRBS13Q Pattern

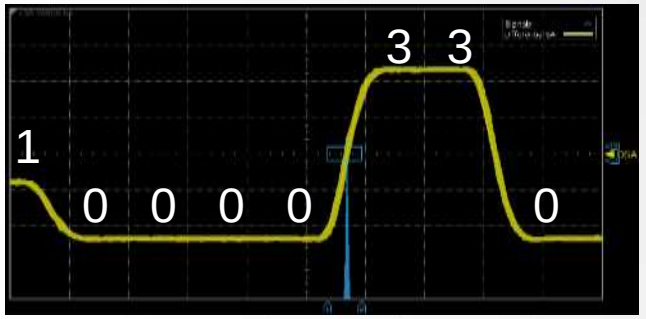
MEASURE J3U, J4U, J-RMS, EVEN-ODD JITTER

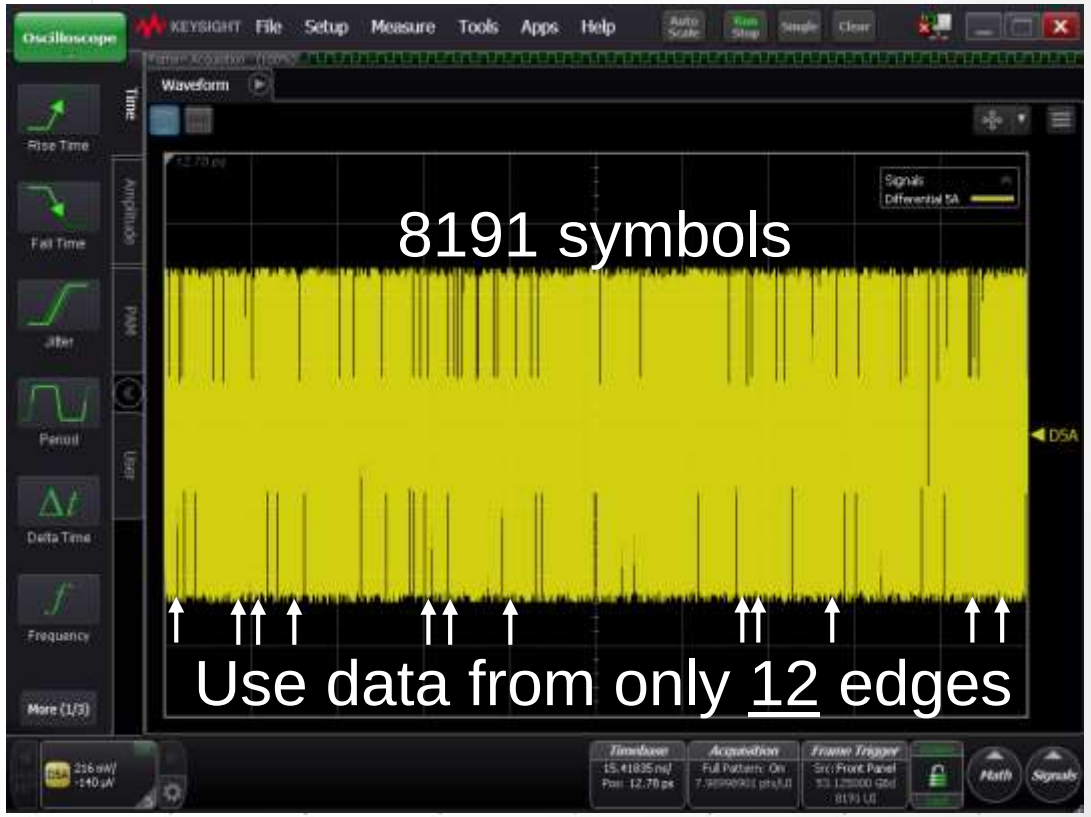
- Output Jitter parameters for Tx:
  - J3u (e.g. IEEE 802.3cd)
  - J4u (e.g. IEEE 802.3bs and CEI-56G-MR/LR)
  - J_{RMS}
  - Even-Odd Jitter (EOJ)

- Measured on 12 specific transitions of a PRBS13Q (IEEE) and QPRBS13-CEI pattern (8191 symbols long) in order to exclude correlated jitter

- 12 transitions represent all possible combinations of 4 identical symbols followed by 2 different identical symbols
  - Captures any jitter issues in Tx design

Example:
- R03 = 10000 330

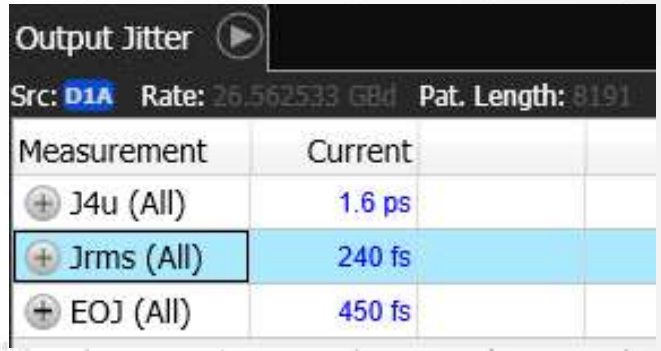


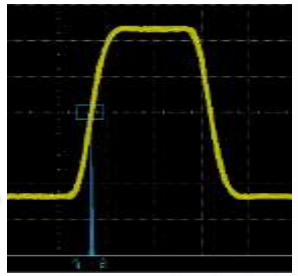


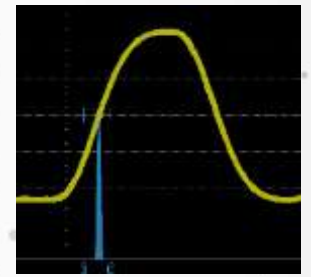
Measurement Considerations/Tips: 12-Edge Output Jitter

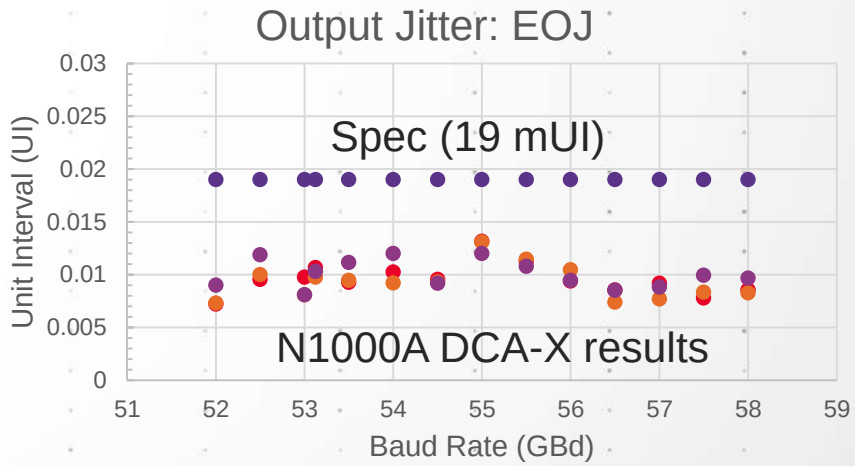
SPEED AND REPEATABILITY

- **Output Jitter (J3u, J4u, J_{RMS}, and EOJ) can be a very time consuming measurement**
  - Requires optimized algorithms
- **Requires a very stable and repeatable timebase**
  - Check for scope repeatability (figure of merit: StdDev)
- **AM-to-PM conversion will impact results**
  - Random noise (RN) will increase measured jitter as channel loss increases (edges will slow down).
  - Expect an increase in J4u, JRMS as channel loss increases.
- **How much data is required for an "accurate" measurement?**
  - RJ/PJ histogram of > 400k typically samples yields stable results
  - Higher channel loss and crosstalk will necessitate more data









Infiniium UXR-Series Real-Time Oscilloscope and N1000A DCA-X Oscilloscope

ENGINEERED FOR TESTING 400G/800G DESIGNS…AND BEYOND

NEW

UXR-Series Real-Time Oscilloscope

NEW

N1000A DCA-X Equivalent-Time “Sampling” Oscilloscope
N1060A Precision Waveform Analyzer (aka “MegaModule”)

Which Scope Should I Use to Characterize PAM4 Signals?

Validation / Verification → Compliance → Troubleshooting

Chip

Board Level

System

Sampling Scopes (SS), "DCA"

✓ **Best for validating/characterizing PAM4 designs**

Real-Time Scopes (RT)

✓ **Best for troubleshooting PAM4 designs**

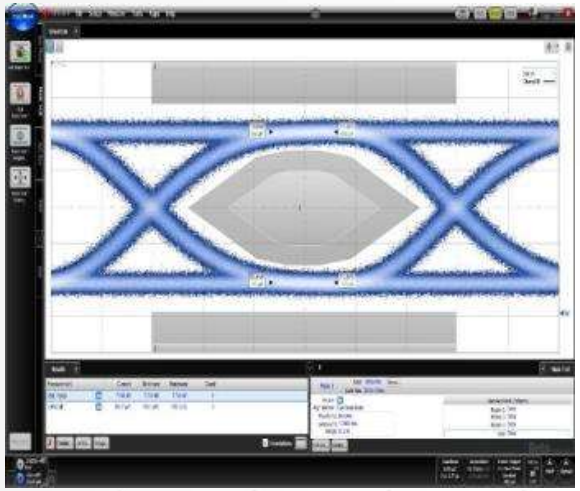
For applications that place top priority on waveform precision:

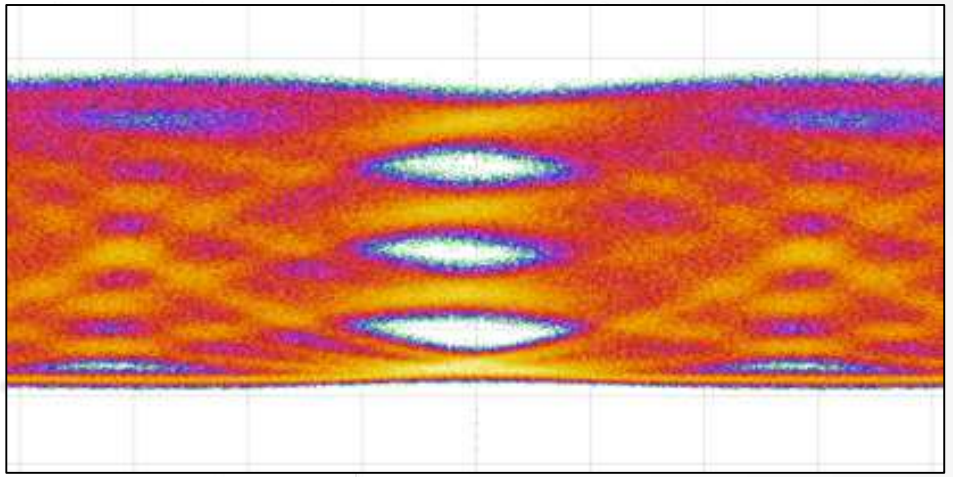
- Highest Fidelity
  - ✓ Low noise
  - ✓ Ultra-low jitter
  - ✓ High Bandwidth
  - ✓ Highest Resolution (16 bits)
- Modular Platform
  - ✓ Electrical/Optical
  - ✓ TDR/TDT
- Lowest price for same BW
- PAM4 Analysis SW
- PAM4 Tx Test "Compliance" SW

The most versatile tool for all areas of high-speed digital communications:

- Best for troubleshooting
- Captures one-time (glitch) events
- No explicit trigger required
- Does not require repetitive signals for pattern waveform measurements
- N7004A Optical-to-Electrical Converter
- PAM4 Analysis SW
- PAM4 Tx Test "Compliance" SW applications
- PAM4 SER/BER "Error Capture" and "Decode"

Key Measurements for Optical Direct Detection Tx

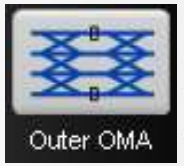


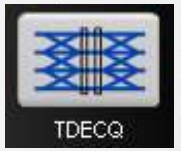


NRZ Transmitters

- **Optical Modulation Amplitude (OMA)** (difference between the 1 level and 0 level)
- **Extinction Ratio (ER)** (ratio of 1 and 0 level)
- **Transmitter Dispersion Penalty (TDP)**
- **Eye-mask**

- **Outer OMA** (difference between the 3 level and 0 level)
- **Outer ER** (ratio of 3 and 0 level)
- **Rise/fall times** (per IEEE 802.3cd)
- **Transmitter and dispersion eye closure for PAM4 (TDECQ)**
  - Replaces mask testing!
  - Requires equalizers and “short patterns” (SSPRQ…no more PRBS31 for TX test).

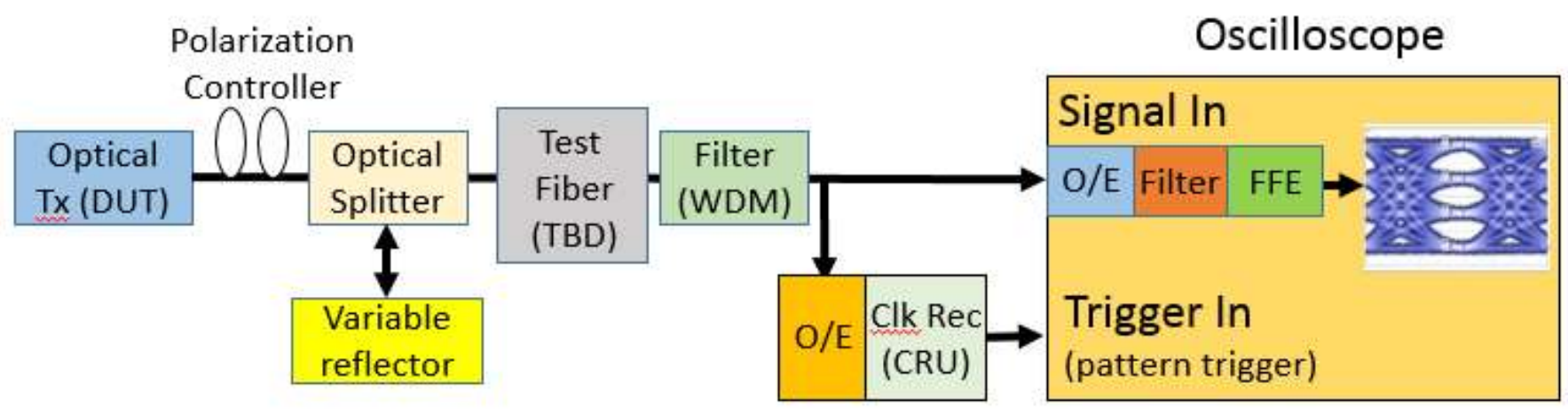




TDECQ

TRANSMITTER DISPERSION AND EYE CLOSURE QUATERNARY

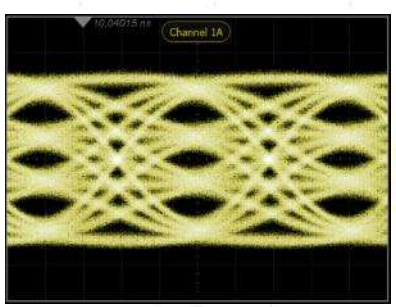
- Tells you the performance of your transmitter relative to an ideal transmitter
- For NRZ TDP, we literally used a BERT to measure the BER performance of the transmitter compared to an actual golden transmitter
  - Determine how much extra power was required at the receiver to compensate for non-ideal performance
- For TDECQ we indirectly measure SER (symbol error rate) using a scope, no BERT required

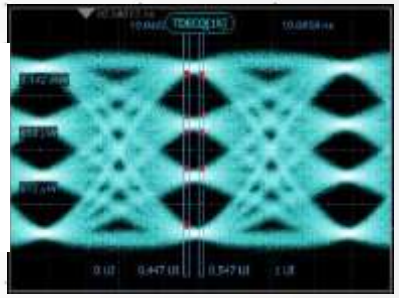


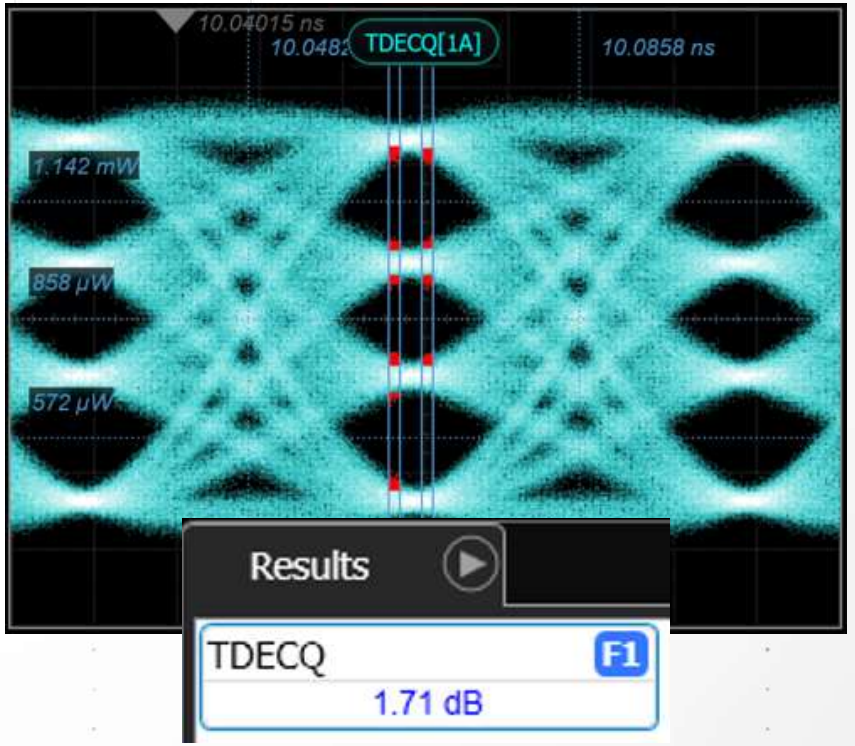
TDECQ Measurement Process

FROM IEEE 802.3BS

- SSPRQ test pattern (2^{16}-1 length)
- Includes test fiber dispersion (single-mode)
- Oscilloscope noise measured and mathematically ‘backed out’
- Apply TDECQ equalizer
  - Virtual 5 tap, T spaced FFE reference equalizer (EQ taps optimized to minimize TDECQ penalty)
- Histograms constructed to assess eye closure relative to OMA and compute an effective power penalty in dB. This is the TDECQ result.
  (note: a smaller number is better)







Keysight Scope Solutions for 26/53 Gbaud Optical Test

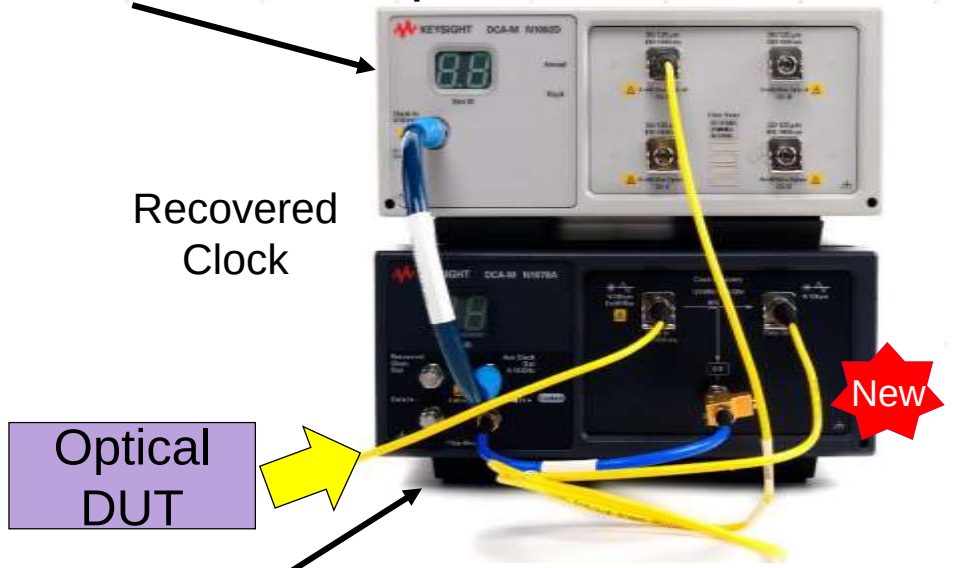
FULLY COMPLIANT FOR ALL OPTICAL PAM4 APPLICATIONS

N1092A/B/D "DCA-M"

- 26/53 GBd Optical Ref Rx
- Multimode and Single-Mode
- 1, 2, or 4 channels
- Low-noise receiver
- PAM4 analysis with TDECQ

N1092x with Optical Clock Recovery

N1092A/B/C/D 26/53 GBd Optical Reference Receiver



N1077A 32 GBd Optical Clock Recovery

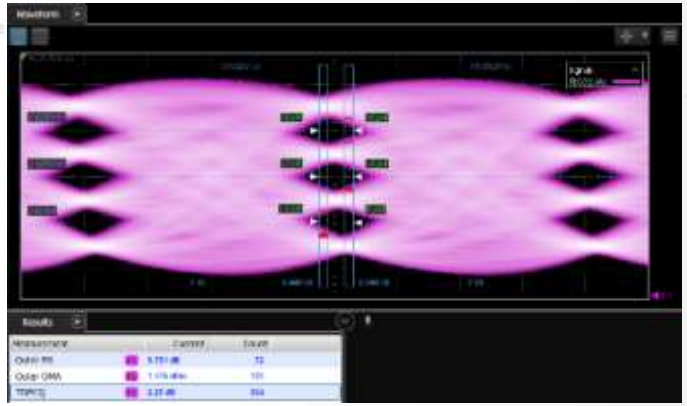
New

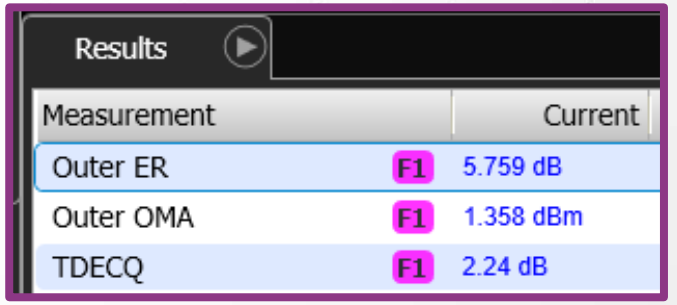
N1078A 64 GBd Optical Clock Recovery

- Includes internal variable equalizer (open "closed" eyes)

FlexDCA User Interface:

- Integrated PAM4 measurements results in FAST, EASY and COMPLIANT measurements





Direct Detect Input (Receiver) Test

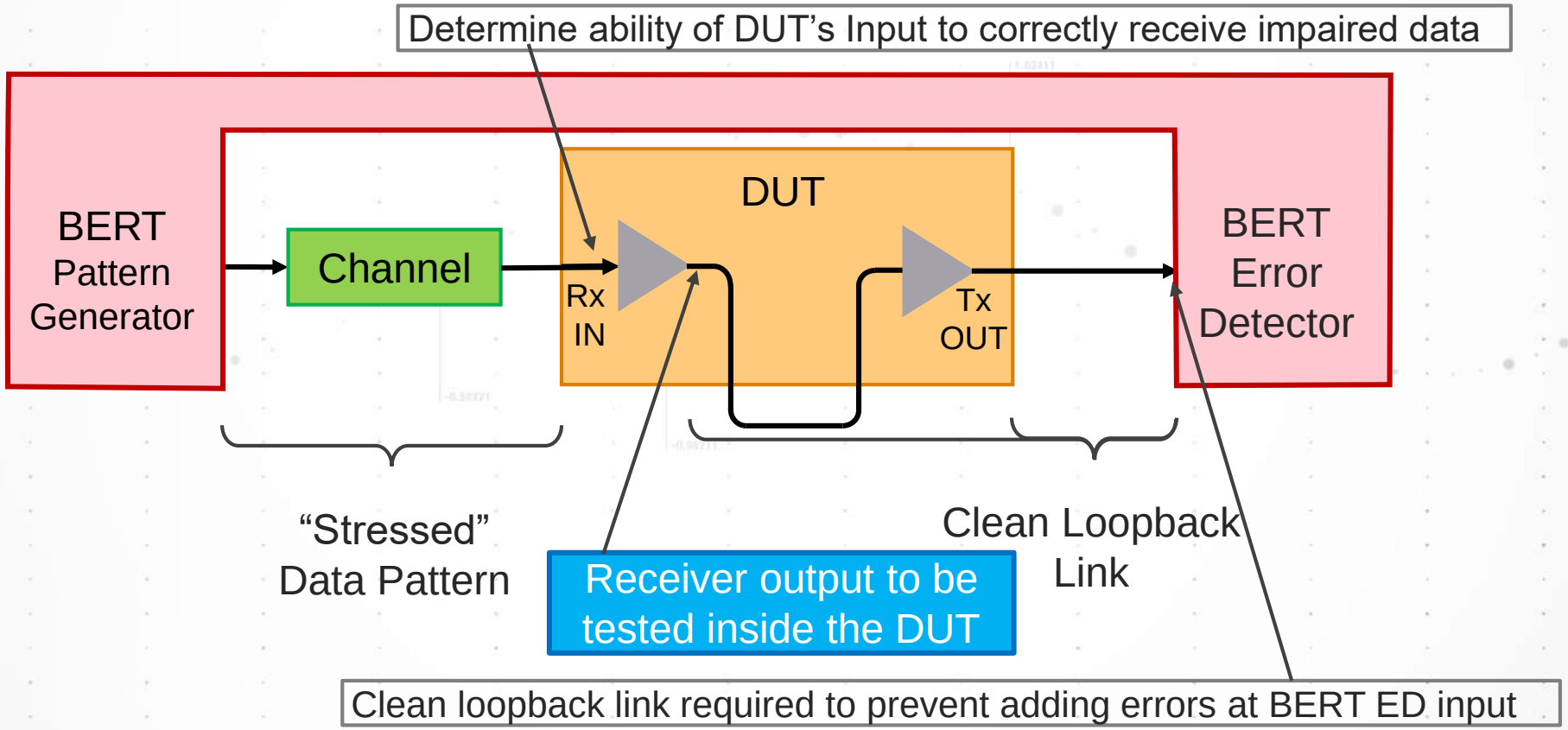
Input Testing Topics

- **Measurement challenges for 56 Gbaud (112 Gb/s) Rx characterization**
  - Links do not run error free (by design) - Avoid use of loopback to BERT ED
  - New reference receiver

Input Testing Links Which Don’t Run Error Free (by design)

- The Bit Error Ratio Tester (BERT) will continue to be the principle tool for input testing

Traditional BERT input test setup

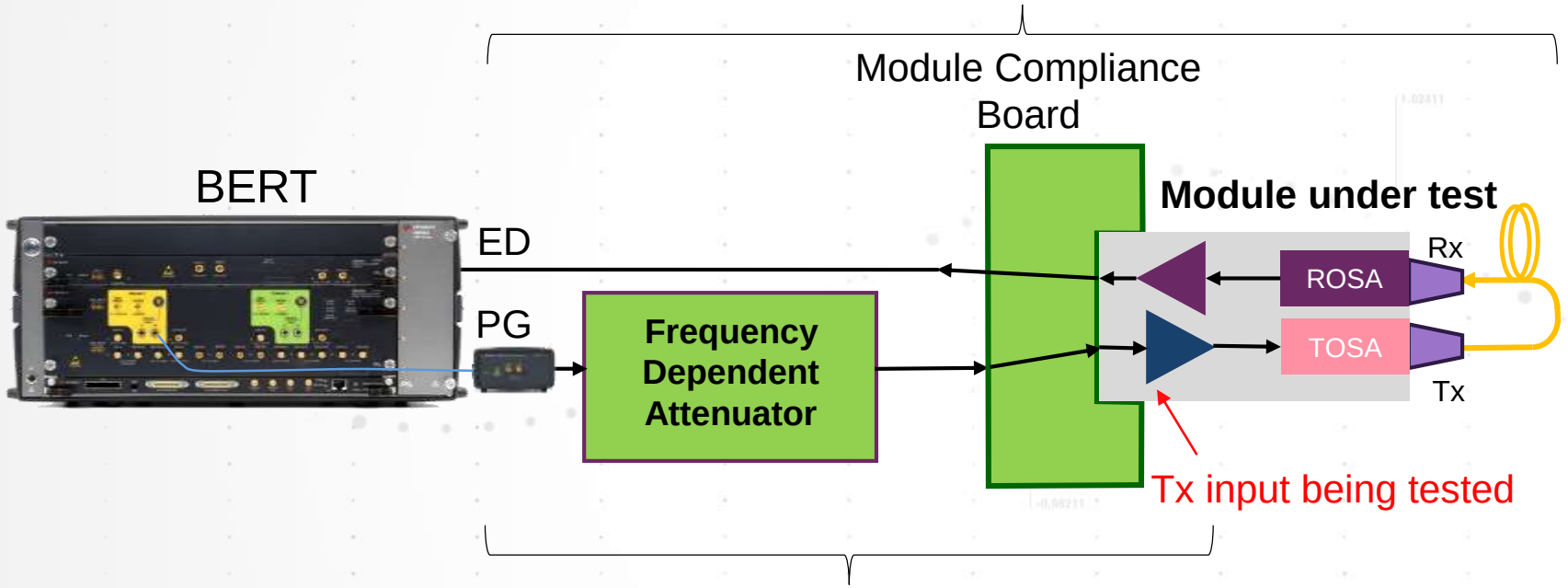


- Will the loopback path be error free in links designed to use FEC for error free operation?

IEEE 802.3 (100G) CAUI-4 C2M Tx Input Test

SAME TEST USED IN LEGACY MODULES (NRZ)

Required BER for entire link (C2M + Optical): 1E-12 (Error free)



1. BERT PG + ISI channel provides stress signal to Tx input
2. Stressed signal drives optical Tx output through TOSA elements
3. Fibre patch cable provides loopback to optical Rx input of same or second (“golden”) module to serve as O/E
4. Looped back signal routed to BERT ED

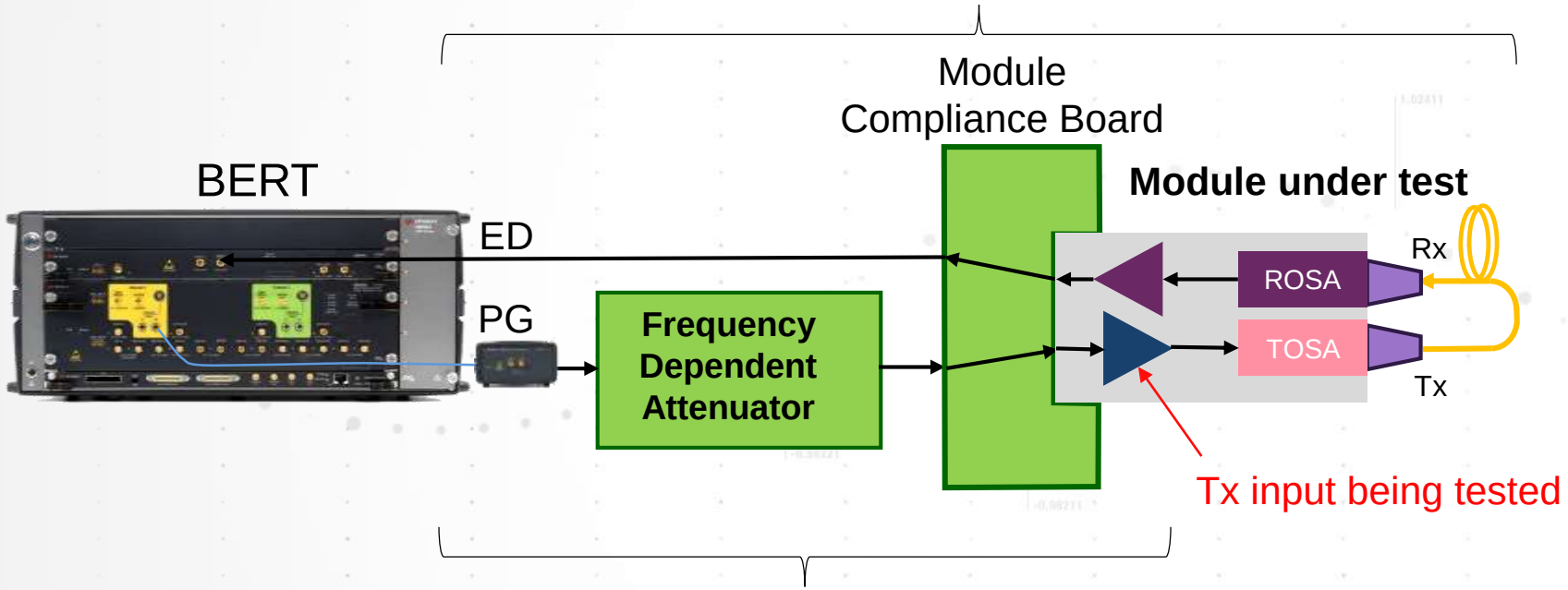
Required BER for CAUI-4 C2M link: 1E-15, tested to 1E-12 (Error free)

Example: 100GBASE-LR4, Tx input (electrical) test, each lane tested independently

400G Requires a Different Test Method

PAM4 LINKS DO NOT RUN ERROR FREE -> REQUIRES FEC

Required pre-FEC BER for entire link (C2M + Optical): 2.4E-4

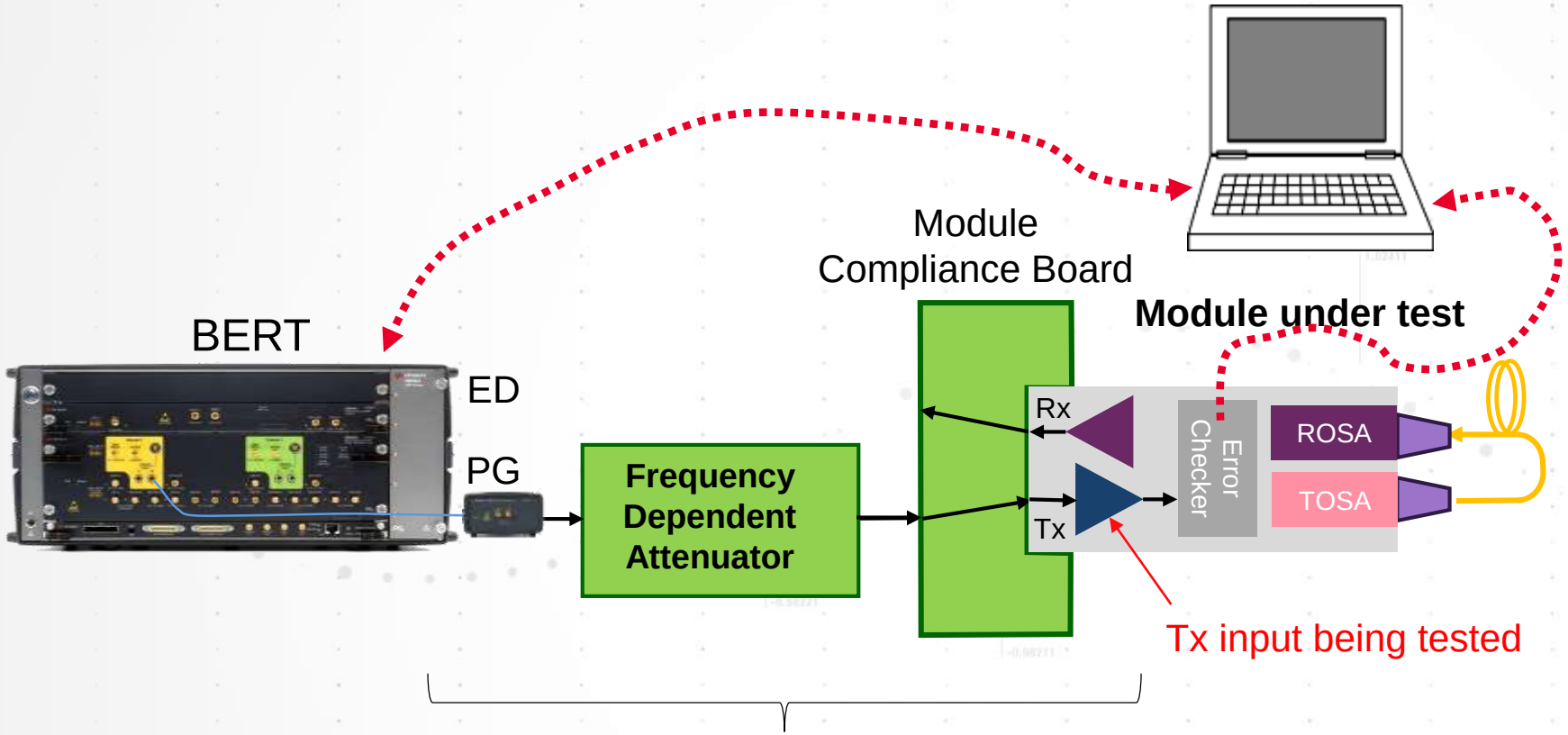


Required pre-FEC BER for 200G AUI-4/ 400G AUI-8 C2M link: 1E-5

Example: 400GBASE-ER8 Tx input (electrical) test, each lane tested independently

- PAM4 links do not run error free
  - ➢ Require Forward Error Correction (FEC) to achieve error free data
- All elements within the link contribute to errors, including the transmitter
  - Distortion, skew, linearity, & noise
- Optical link has worse BER than C2M electrical link under test – should not be used as loopback path
- Errors at the BERT ED input will be added to actual errors detected from the Tx input under test – over stating the BER

Preferred Input Test Method When Loopback Path is PAM4



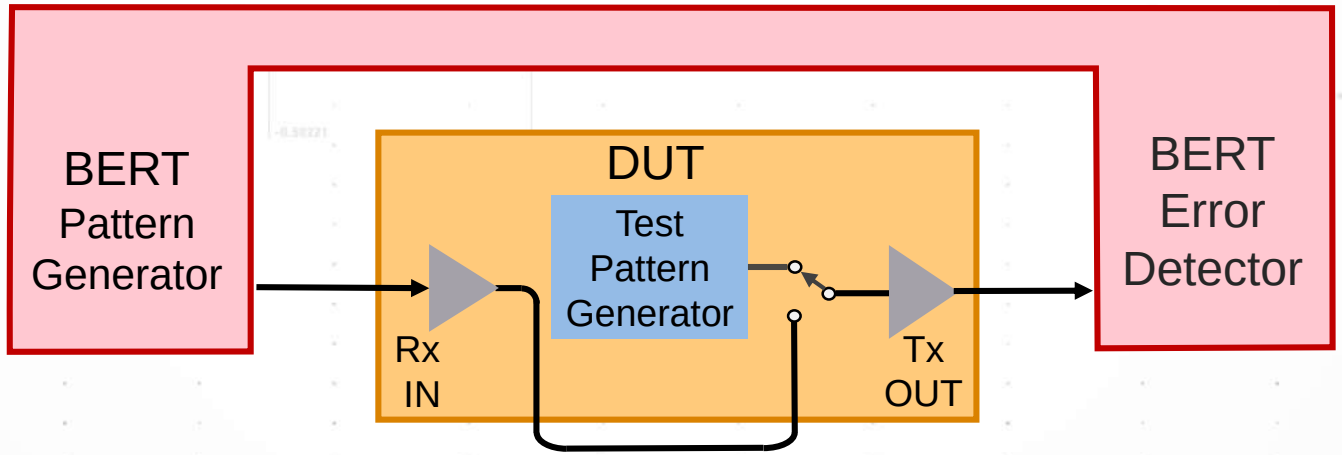
Required BER for 200G AUI-4/ 400G AUI-8 C2M link: 1E-5

Example: 400GBASE-ER8, each lane tested independently

- When error free loopback link cannot be assured (as in PAM-4 links), an internal error checker directly driven by input receiver under test should be used for accurate BER measurements
- BERT is still used to generate stressed test pattern, but not for error detection
- Error checker in DUT is read through alternate link, such as the management interface
- Data from DUT error checker can be read into Keysight M8070B System Software for M8000 BER test Solutions to enable direct JTOL and other measurements, identical capabilities as those made with BERT error detector

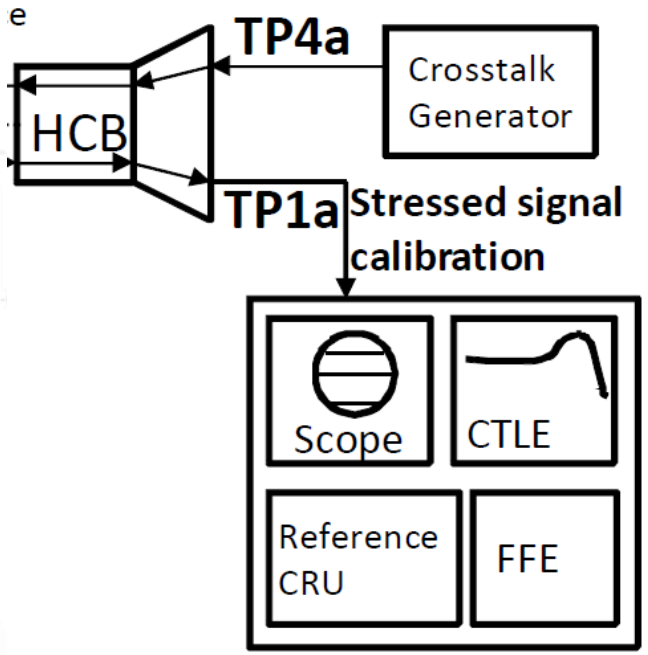
Chip Design Considerations for Receiver Testability

- Use of internal error checkers eliminates degraded BER measurements from loopback path errors
  - PRBS31Q (same as OIF QPRBS31-CEI) is the standard test pattern for C2M compliance input testing
- If chip density does not allow internal error checker, consider adding PRBS-Q pattern generator
  - Pattern generator provides means to measure BER in loopback path only, isolated from receiver under test



Challenges With Proposed Reference Receiver

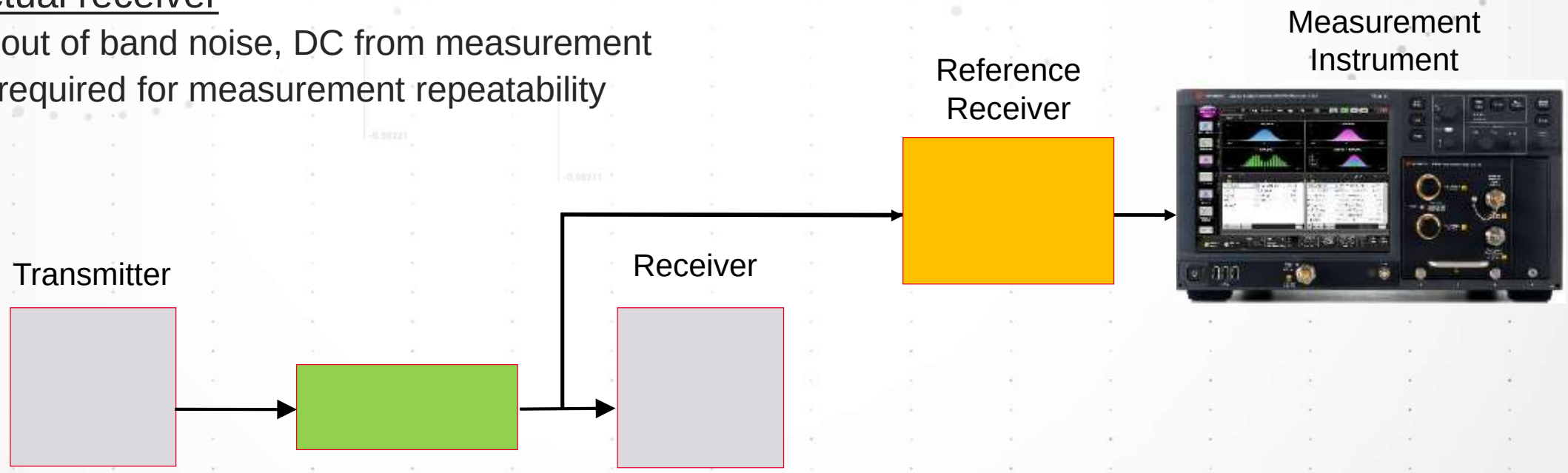
- The “Reference Receiver’ normalizes the signal conditioning front end in test instruments used for Output (Tx) measurements and Input (Rx) stressed eye calibration
- Reference receiver is supposed to emulate a generic receiver implementation with minimal performance required to close the link budget



Reference: OIF CEI-112G-VSR Figure 23-10 Module Input Test Setup Draft ver. 07

Why is the Reference Receiver Needed?

- Problem – measurement instrument may “see” artifacts in the link signal that will not impact the receiver
  - e.g. higher frequency components beyond receiver bandwidth
- Solution – add a “Reference Receiver” to constrain measurement to signals as seen by actual receiver
  - Removes out of band noise, DC from measurement
  - Accuracy required for measurement repeatability

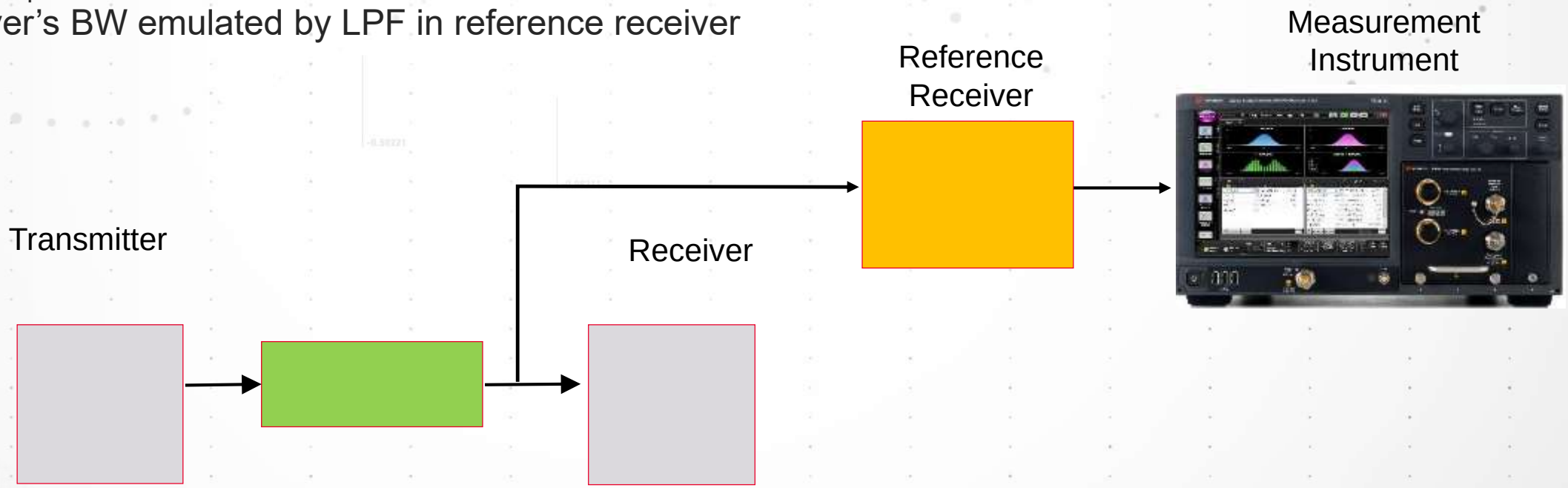


The Reference Receiver

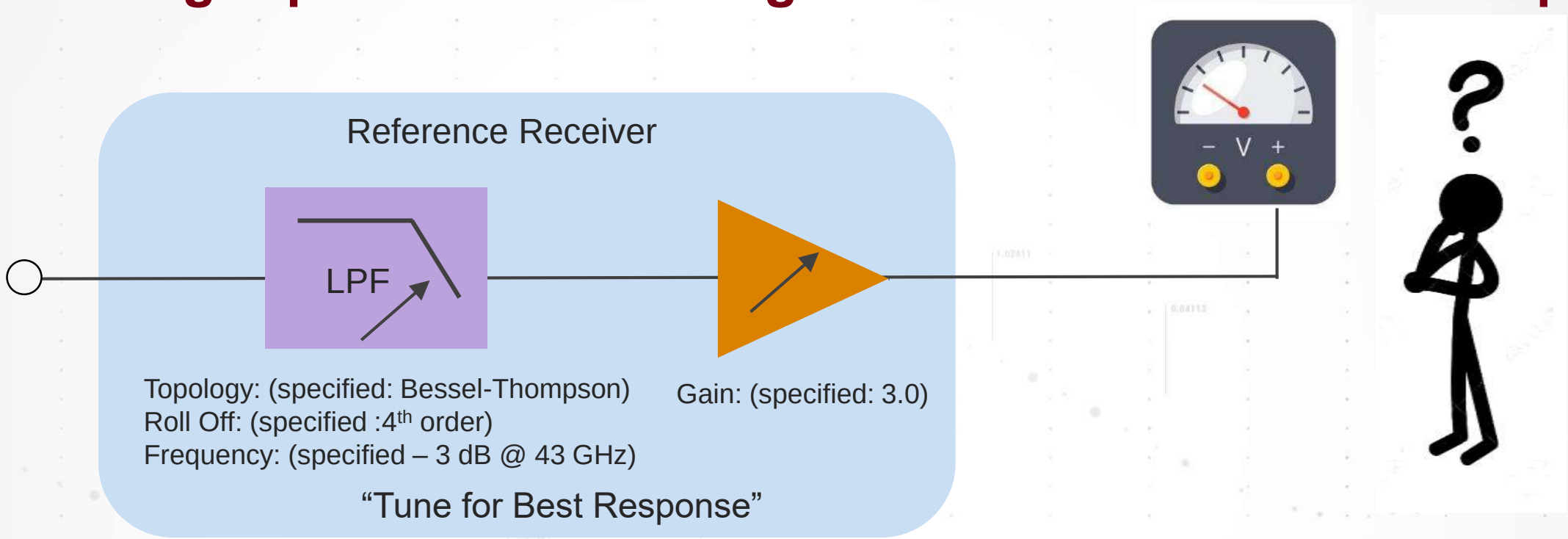
- Accurate measurement of what the DUT is seeing, results when reference receiver uses this approximation:

$$H_{DUT\ par.}(x) = H_{Ref.Rec.}(x)$$

- Where $H_{DUT\ par.}(X)$ is the actual receiver response to the parameter being measured
  - e.g. receiver's BW emulated by LPF in reference receiver



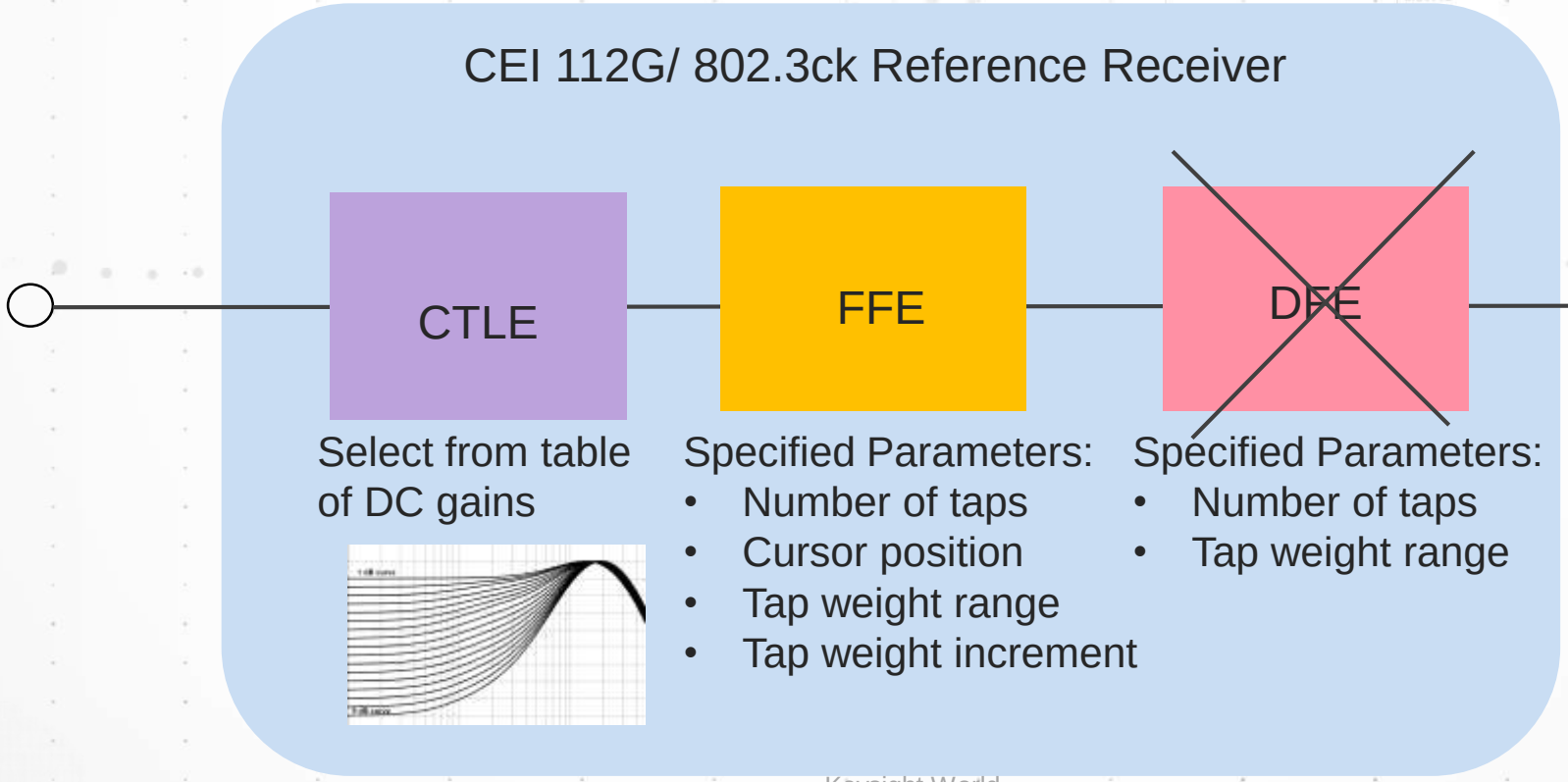
Optimizing Equalizers – Challenge Reference Receiver Concept



- Traditionally, operational parameters of signal conditioning in front of test instrument are tightly specified for repeatable measurements
- Optimizing equalizer ("Tune for best response")
- OK for receiver, but challenges measurement repeatability
  - Example – self optimizing equalizer gives 50% UI EW in one case, with same Tx and channel, 58% in another. Fine for a real receiver, but not a measurement instrument ! (16% difference in EW measurements)

Current Equalizer Proposal

- Cascaded equalizer – CTLE + FFE and possibly DFE
- All stages are self optimizing



Measurement Instrument

How to Make Self Optimizing Equalizer in RR Repeatable?

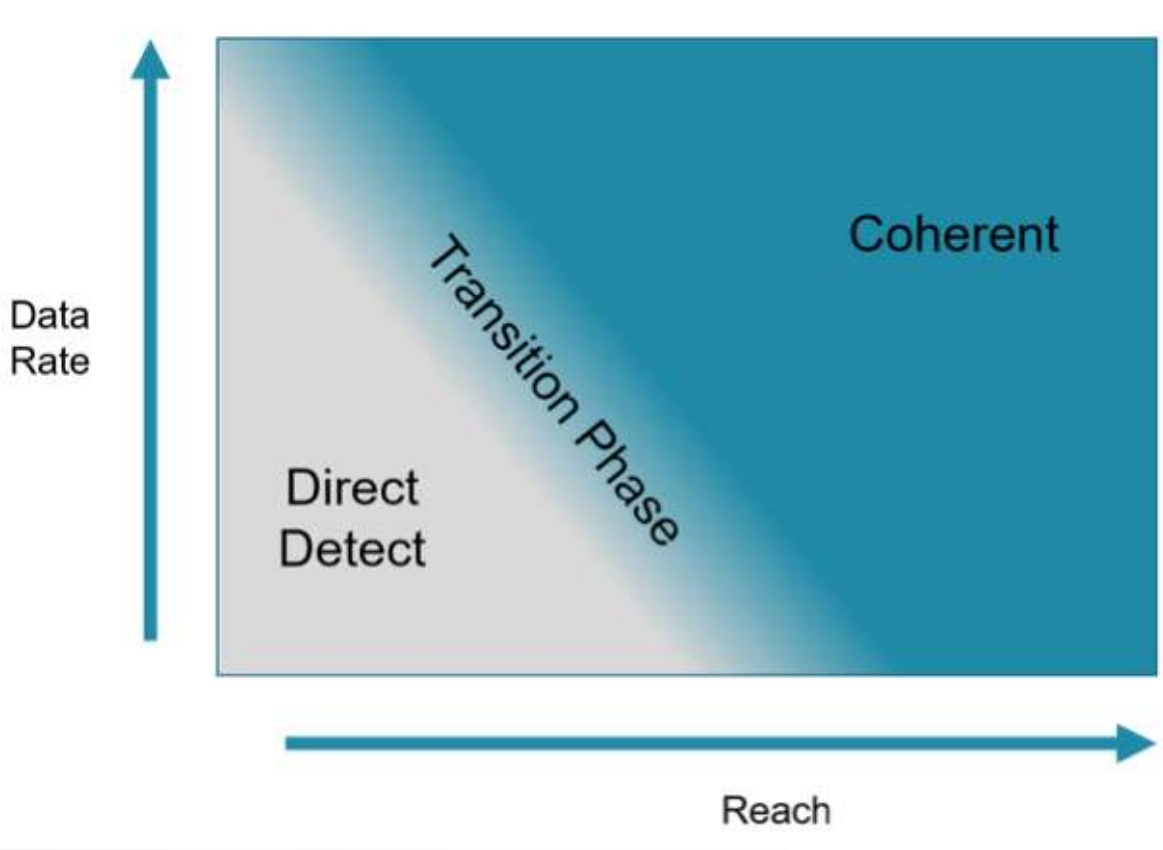
In theory optimizing equalizers could be used in reference receivers and give repeatable measurements when these conditions are met:

- Order of placement of equalizer elements (CTLE first, followed by DFE or FFE, followed by ___)
  - Linear systems should allow interchanging, but this ignores action of noise on individual equalizer elements
- Tap configuration
  - Cursor placement
  - Lange limits
  - Increment step size
- Optimization stop criteria
- Will actual implementations follow theory and be repeatable?
  - Concern with recent example – TDECQ measurement (output Tx output in 400G 802.3cd standard project)
  - TDECQ algorithm required several draft iterations to address non-repeatability between instrument vendors and poor correlation with BER results
  - Large cause was found in self-optimizing TDECQ equalizer (FFE), and Ref RX model was not representative of actual RX

Coherent Optical Test

Coherent Moves into the Data Center

COHERENT VS DIRECT DETECTION: A COST AND POWER GAME



Source: Acacia Inc.

Direct Detection (PAM4)

Cost

Power / Size

Latency

Needs CD compensation depending on link length

Bandwidth (DWDM): 4 Tbit/s

Coherent

Cost

Power / Size

Latency

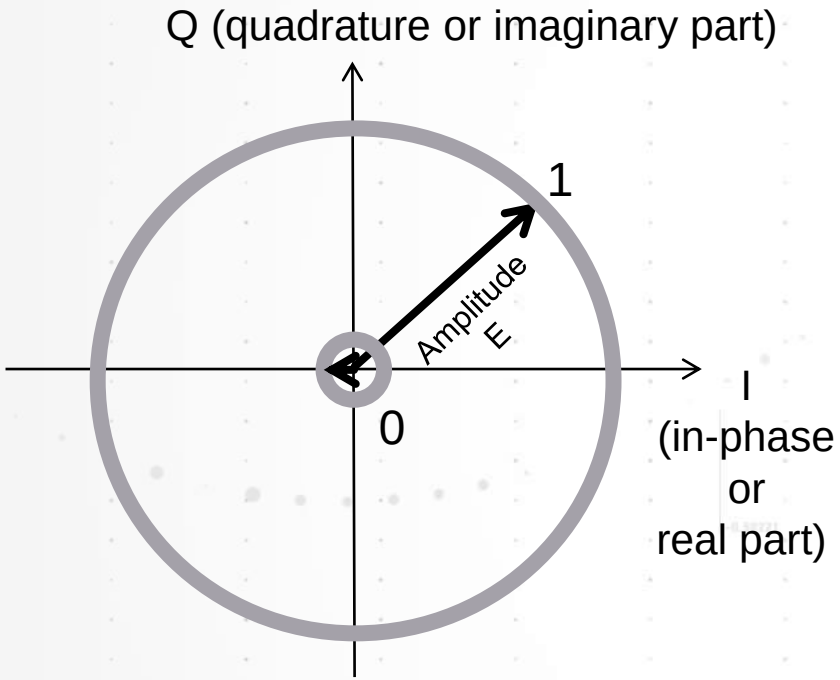
} Being addressed through reducing DSP requirements and moving to 7 nm CMOS

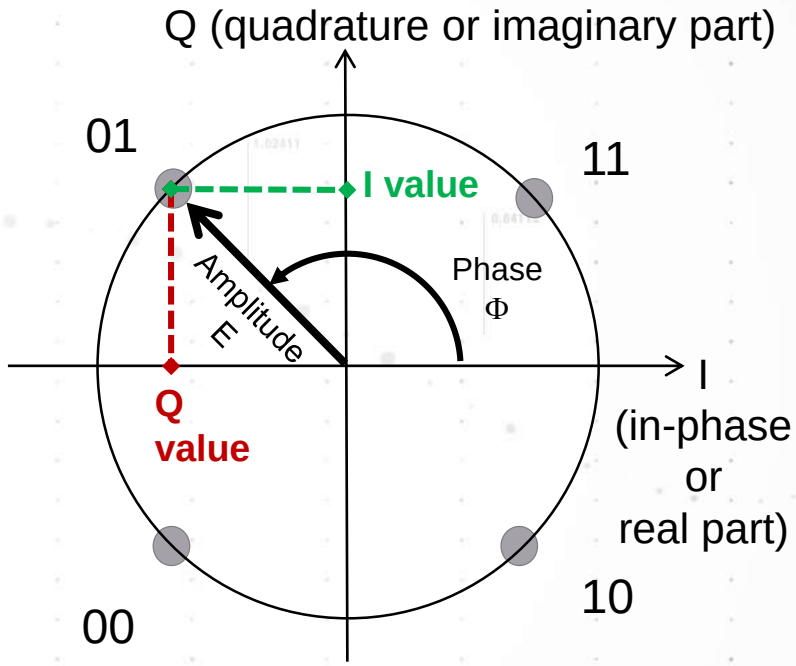
DSP compensates CD adaptive to link length

Bandwidth (DWDM): 20 / 30 Tbit/s with 16 / 64QAM

ON-OFF-Keying (OOK) vs. Digital Complex Modulation

GRAPHICAL REPRESENTATION



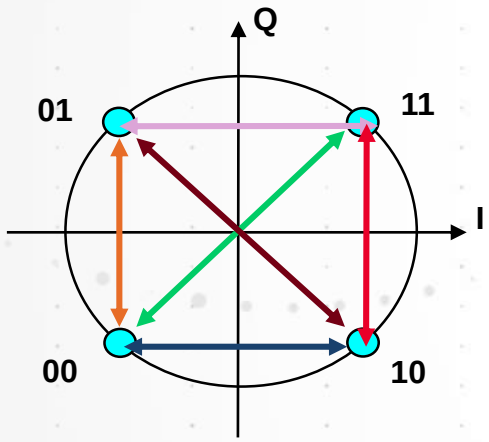


1) Information is in amplitude
2) Phase can be random

1) Information is in amplitude
2) Information is in phase

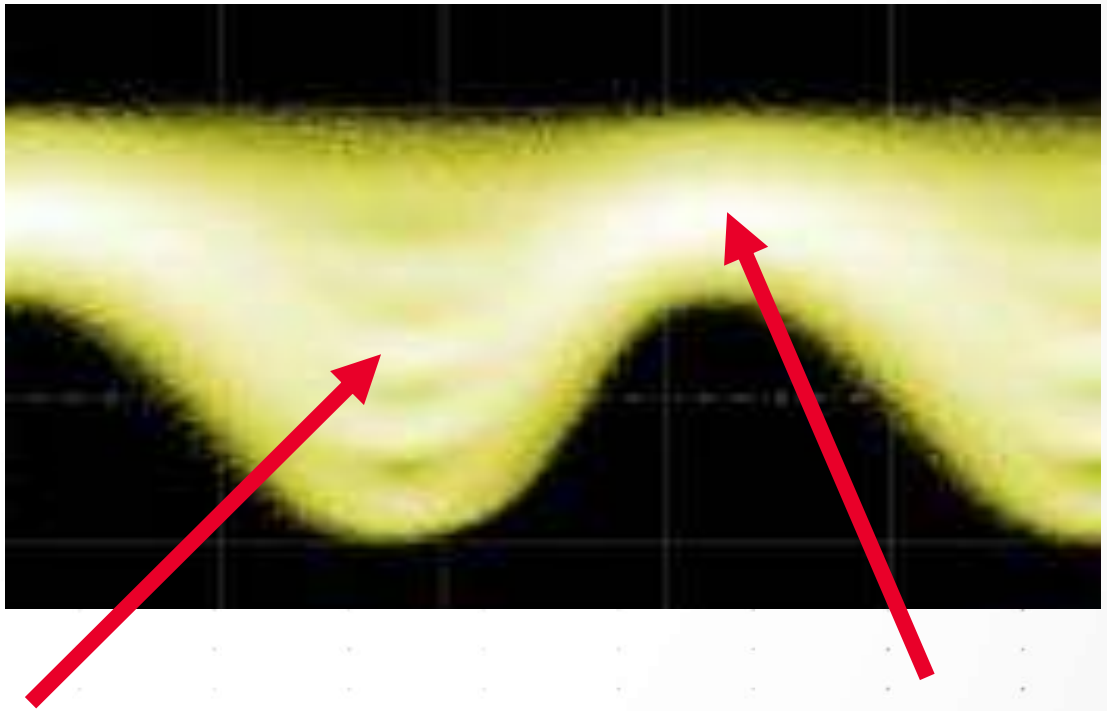
Analyzing Complex Modulated Signals with Conventional Direct Detection Methods?

Q (quadrature, imaginary part)



I (in-phase, real part)

QPSK constellation map



This is the region of transition between symbols

This is the region where the symbol/vector state should be stable and where communications quality is assessed

Need amplitude AND phase sensitive measurement!

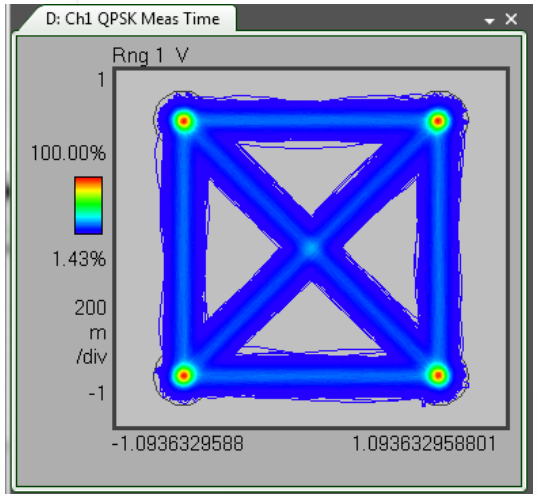
Different Metrics Required for Direct Detection and Coherent Transmitters

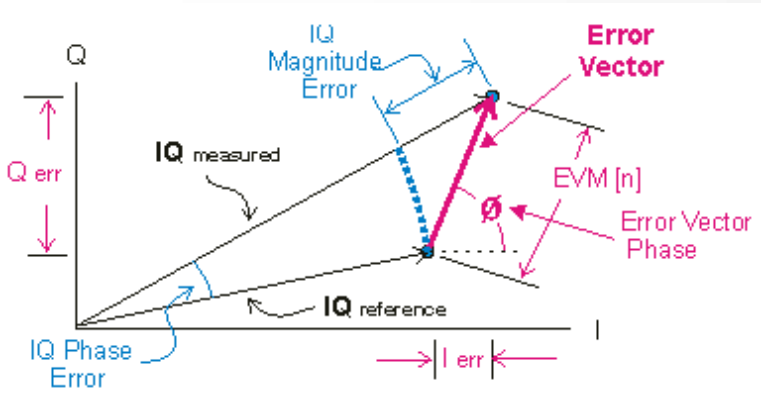
OOK (NRZ / PAM4)

- Q-factor
- Eye mask (NRZ)
- TDECQ (PAM4)
- Timing jitter
- BER
- OSNR

Complex Modulation

- EVM
- IQ Imbalance, IQ Offset
- Quadrature Error
- Frequency Offset
- BER
- OSNR



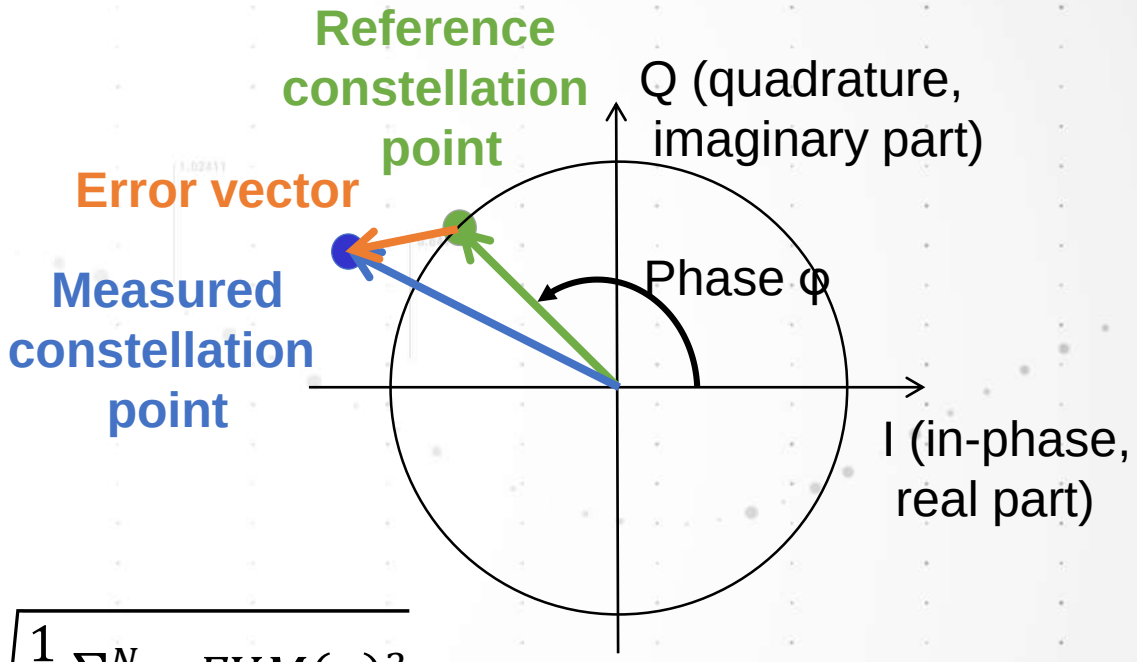


Error Vector Magnitude

QUALITY MEASURE FOR COMPLEX MODULATED DATA SIGNALS

✓ Global quality metric for coherent Tx

- Needs reference receiver comprising
  - Calibrated optical front-end
  - Real-time ADC
  - Defined signal processing blocks



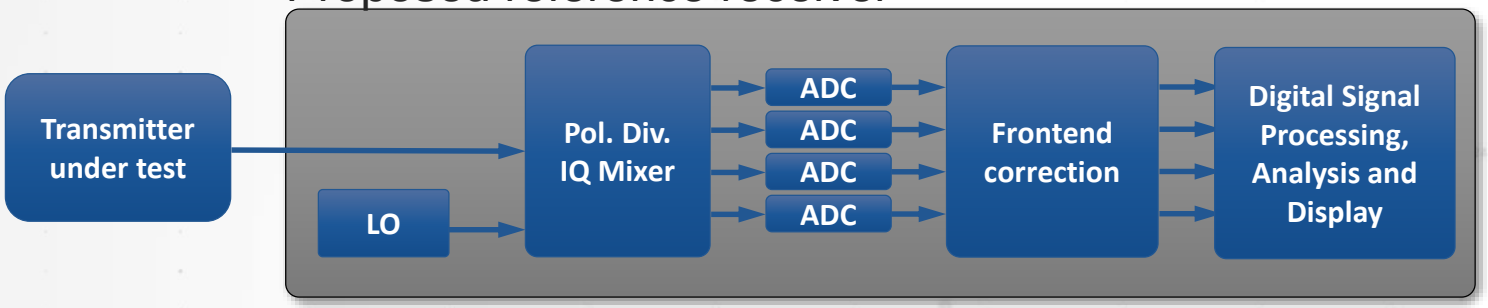
$$EVM_{rms} = \frac{\sqrt{\frac{1}{N}\sum_{n=1}^{N} EVM(n)^2}}{|peak\ ref.vector|}$$

The Error Vector connects the measured vector and the reference vector!
An Error Vector = 0 means we have an ideal signal!

Method to Determine EVM

ADDITIONAL IMPAIRMENT ANALYSIS FEATURES

Proposed reference receiver



M8290A

- ✓ **Optimized for up to 400G signals**
- ✓ **Most compact**
- ✓ **Most affordable**
- ✓ **4ch. 92 GSa/s**
- ✓ **40 GHz**
- ✓ **512 kSa memory**

Proposed reference receiver for coherent transmitter testing:

- Dual-polarization coherent receiver
- Real-time signal acquisition (four synchronized ADC channels)
- Frontend correction
- Digital signal processing

Reference receiver HW & SW characteristics need to be specified for the development of an EVM specification

Keysight supports these efforts in:

ITU OIF IEEE

Outlook

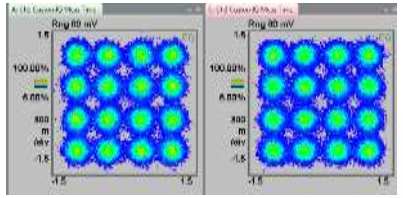
LOOKING TOWARDS 800G

- First vertically integrated non-interoperable solutions announced by Infinera and Ciena
  - Transmission rates from 100G to 800G
  - Up to 100 Gbaud symbol rate
  - Advanced signal processing methods like probabilistic constellation shaping and Nyquist sub-carriers
- Second generation of 800G solutions expected for 2021
  - Lower power consumption
  - Lower footprint
  - Interoperable

- The test equipment is ready

N4391B OMA
- ✓ **4ch. 256 GS/s**
- ✓ **40 – 110 GHz BW options**
- ✓ **200MSa – 2 GSa memory**
- ✓ **Lowest noise floor**
- ✓ **Lowest skew**

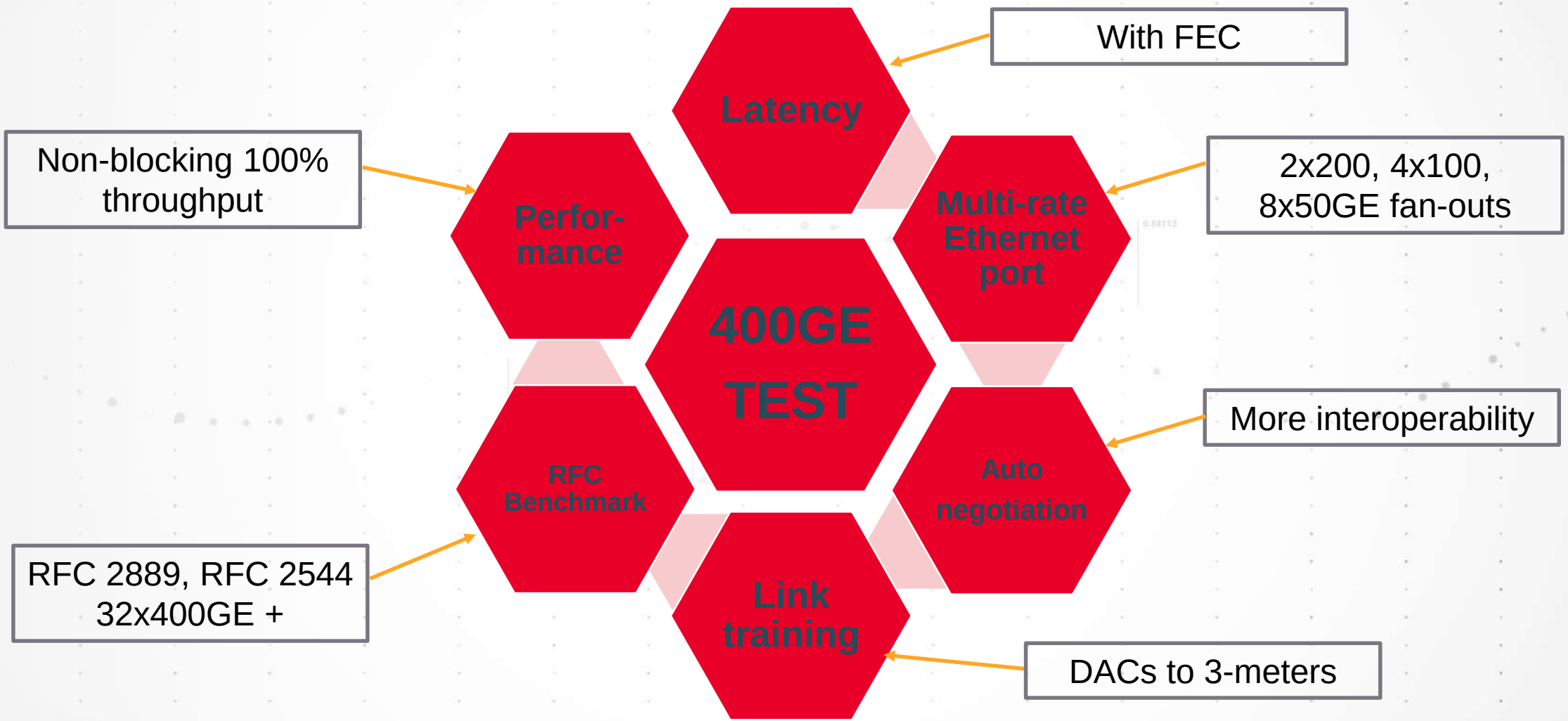
M8194A AWG
- ✓ **4ch. 120 GSa/s**
- ✓ **> 45 GHz 3-dB bandwidth**
- ✓ **Signal generation up to 50 GHz**
- ✓ **512 kSa memory**



DP-16 QAM constellation at **100 Gbaud**
Optical measurement

Layer 2-3 Test

400G (PAM4) Changes What Needs to be Tested…



FEC Analysis is Critical

400GE STD, FEC, WHAT TO LOOK FOR

- Forward Error Correction (FEC)
  - Corrects errors on the Receive side (Goal: no packet errors)
  - FEC corrects up to 15 symbol errors per code word
  - An uncorrectable code word results in equivalent of ~15 64B packets

CRITERIA

Pre FEC BER 10^-4

Frame Loss Ratio

No uncorrectable code words

HEALTHY?

Look beyond “lack of CRC errors”, pre FEC BER & FLR

Review how close to the limit of FEC

Monitor error distribution per physical lane

Monitor symbol error density

FEC Total Bit Errors	1,685,086,529
FEC Max Corrected Symbols	15
FEC Corrected Codewords	787,415,758
FEC Total Codewords	8,747,730,910
FEC Frame Loss Ratio	0.00e+000
pre FEC Bit Error Rate	3.54e-005
FEC Codeword with 0 error	7,960,315,152
FEC Codeword with 1 error	551,108,911
FEC Codeword with 2 errors	200,069,411
FEC Codeword with 3 errors	26,209,344
FEC Codeword with 4 errors	8,176,726
FEC Codeword with 5 errors	1,363,216
FEC Codeword with 6 errors	382,557
FEC Codeword with 7 errors	77,640
FEC Codeword with 8 errors	21,150
FEC Codeword with 9 errors	4,968
FEC Codeword with 10 errors	1,349
FEC Codeword with 11 errors	356
FEC Codeword with 12 errors	93
FEC Codeword with 13 errors	26
FEC Codeword with 14 errors	8
FEC Codeword with 15 errors	3
FEC Uncorrectable Codewords	0

Introducing ARESONE-400GE

3.2
Tbps

2RU
Fixed Chassis

56 Gb/s
PAM4 Encoding/ Decoding

Multi-Speed
400/200/100/ 50GE

Protocol testing

QSFP-DD
OR
OSFP

Summary

Summary - Keysight Provides Industry Leading Tools

FAST AND ACCURATE CHARACTERIZATION OF PAM4 DESIGNS

M8040A BERT

M8194A AWG

Receiver

N1000A DCA-X / N1092A DCA-M
Sampling Scope

UXR Real-time Scope

Transmitter

ARESONE-400GE

L2/L3 400GE Test

400G Design Cycle

PLTS + M980Xa VNA

Channel/ Interconnect

Modeling / Link Simulation

ADS, FlexDCA link

Questions?

Please stop by the demo booth

Data Center / Telecom Track Demos

SEE AND HEAR THE LATEST AND GREATEST FROM INDUSTRY EXPERTS

PCIe 5.0 Tx

Signal Quality at PCIe 5.0 Speed

Highest Signal Integrity at 32 GT/s

Measure Highest Design Margins

Simple Measurement Execution

PCIe 5.0 Rx

Validating 32 GT/s Receivers

Automated Rx Calibration

Protocol Aware at 32 GT/s

Interactive Link Training

DDR5 Tx

Double the Speed of DDR4

Complete Integrated Workflow

Probe for Easy Signal Access

Automated Test & Reporting

DDR5 Rx

Verify DDR Receivers at 6 Gb/s+

Full Speed & Accuracy

Only Rx Compliance Test Solution

Signal Integrity

Signal Distortion at 400G Speeds

Precision 400G Measurements

Extreme Bandwidth Over Copper

End-to-end Characterization

Memory Design

Tedious Design/Test Cycles

Unified Design and Test

DDR Memory Designer

Test Plan Automation

400G Tx / Rx

Moving from 400G to 800G and beyond

Accurate 400G/800G measurements

Full Tx Compliance testing of 400G designs

Full PAM4 Signal Analysis

400G Network Validation

Ensure 400GE Performance

Verify QSFP-DD/OSFP

Test 200/100/50GE

Interoperability


KEYSIGHT
WORLD 2019

Acronyms

c2c = Chip-to-Chip
c2m = Chip-to-Module
BER = Bit Error Ratio
BUJ = Bounded Uncorrelated Jitter (used to emulate crosstalk)
DUT = Device Under Test
EW = Eye Width
EH = Eye Height
FEC = Forward Error Correction
FFE = Feed-Forward Equalizer
NRZ = Non-Return to Zero (Refers to 2 level signaling or PAM-2)
PAM-*n* = Pulse Amplitude Modulation, where *n* = number of levels
RJ = Random Jitter
RS = Reed Solomon
SER = Symbol Error Ratio
SIRC – System Impulse Response Correction
SJ = Sinusoidal Jitter
SMF/MM F– Single-mode fiber, Multimode fiber
TDP = Transmitter and Dispersion Penalty
TDEC = Transmitter and Dispersion Eye Closure
TDECQ = Transmitter and dispersion eye closure quaternary (for PAM4)