KEYSIGHT WORLD 2019

USB Type-C™ Future Technologies and Solutions

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Keysight Technologies

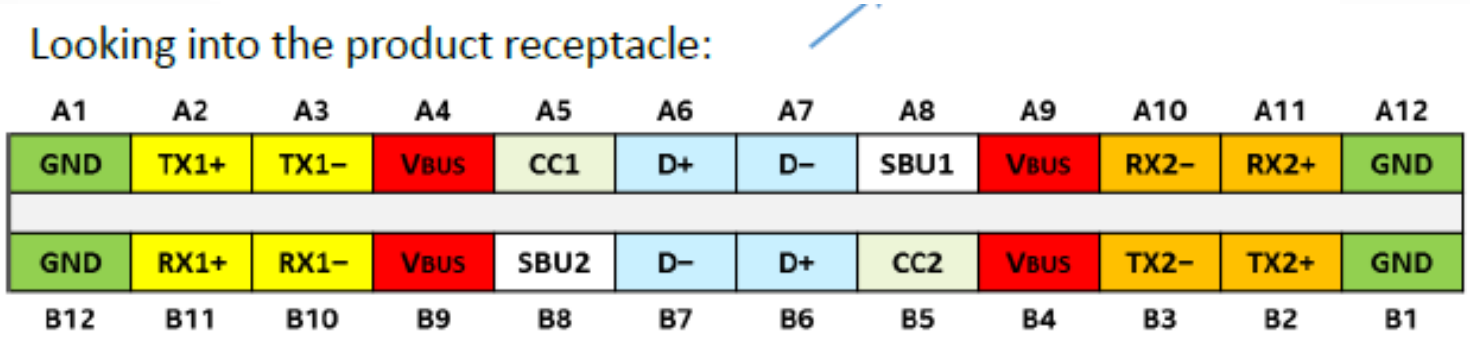
Agenda

- Technology Waves
- Fundamental Challenges
- USB 3.2 Retimer
- USB 3.2 Redriver
- USB 3.2 x2
- Introduction to USB4
- What happens after USB4?
- eUSB2 Overview
- Summary
- Q&A

Publicly Announced Technology Waves

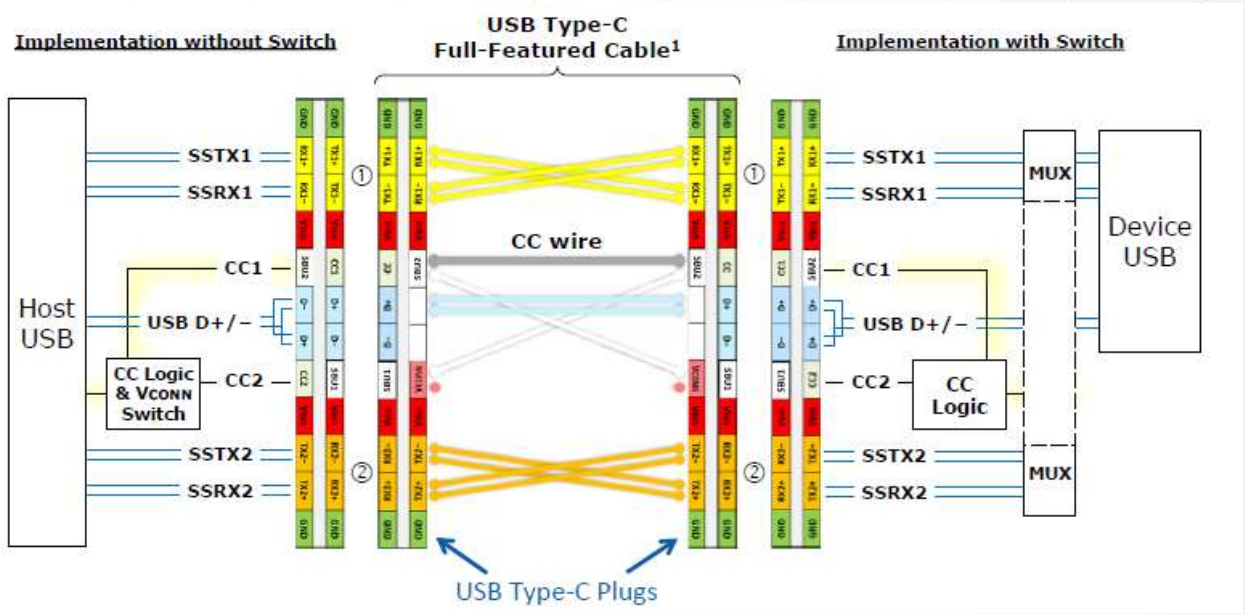
- USB-IF releases USB 3.2 x2 and Retimer Specification
- Ice Lake processor will be first to integrate Thunderbolt 3: https://newsroom.intel.com/news/intel-takes-steps-enable-thunderbolt-3-everywhere-releases-protocol/#gs.b2jb5k
- USB-IF proposing Redriver Cable Test Specification
- USB-IF announces USB4:

  https://usb.org/sites/default/files/2019-03/USB_PG_USB4_DevUpdate_Announcement_FINAL_20190226.pdf

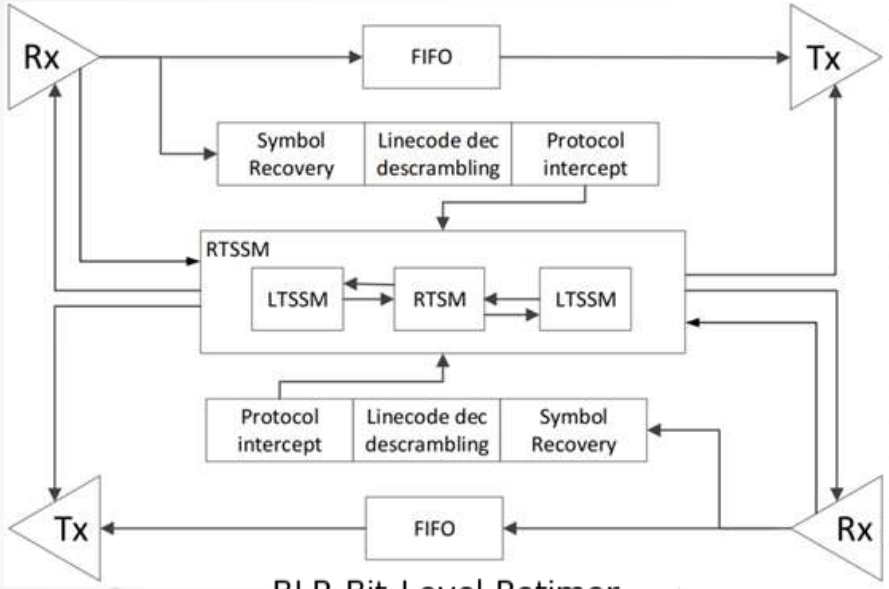


Fundamental Challenges

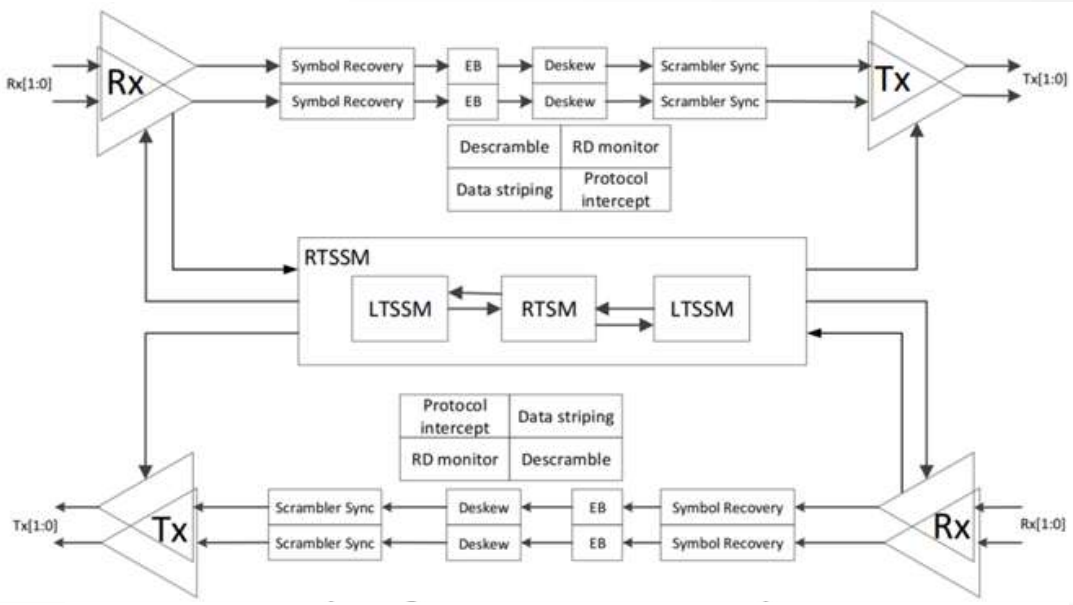
- Thunderbolt/USB integrated CPU
  - Channel lengths for 10/20 Gbps signaling will be much longer.
- X2 mode
  - Comprehend crosstalk
- Repeater
  - SRIS retimer
  - BLR retimer
  - Redrivers
- USB4 Open Spec
  - PHY rate doubled to 20 Gbps, x2 mode doubles that to 40Gbps



USB 3.2 SRIS and BLR Retimer Overview



BLR Bit Level Retimer



SRIS

Separate Reference clock

Independent SSC Retimer

- Bit Level Retimer
  - TX Clock derived from incoming Clock Data Recovery
- Separate Reference Clock Independent Spread
  - Clock offset compensation via Elastic Buffer

USB 3.2 SRIS and BLR TX Testing

- Component
- Embedded
- BLR Compliance Mode
- PassThrough Loopback Mode
- SKP OS CPx Toggle
- Dual PG for Compliance Mode Entry and CPx Toggle
- Stressed LTSSM propagation and signaling
- Clock Switch dF/dt test
- Jitter Transfer Function test

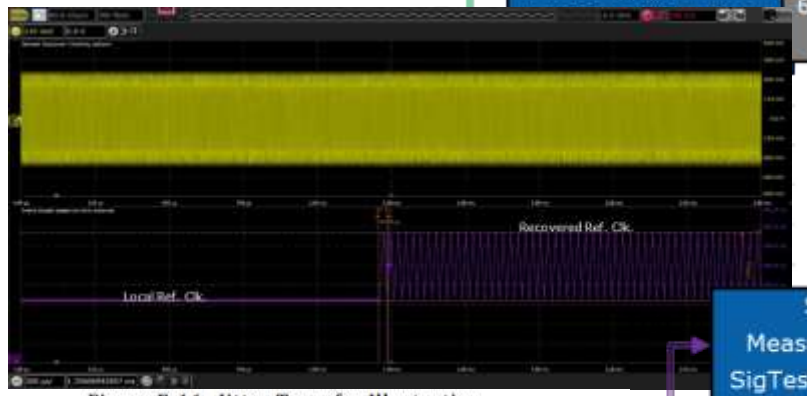


Figure E-16. Jitter Transfer Illustration

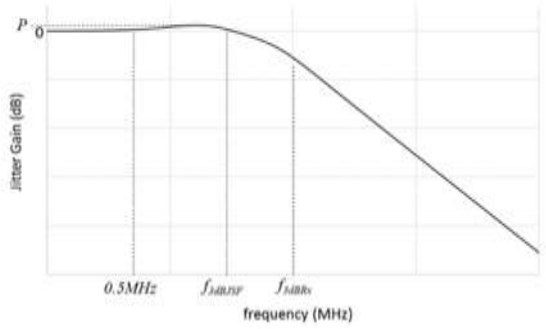
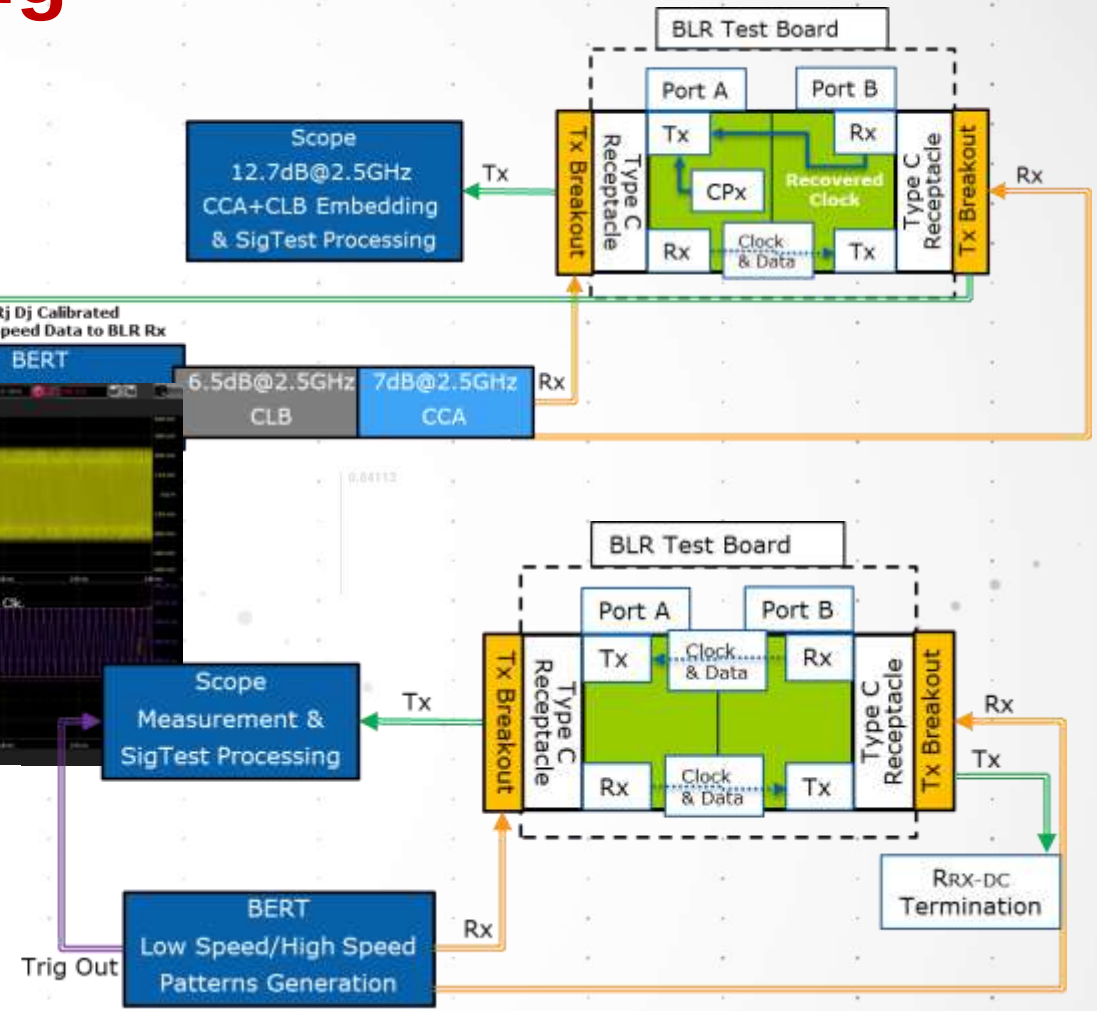


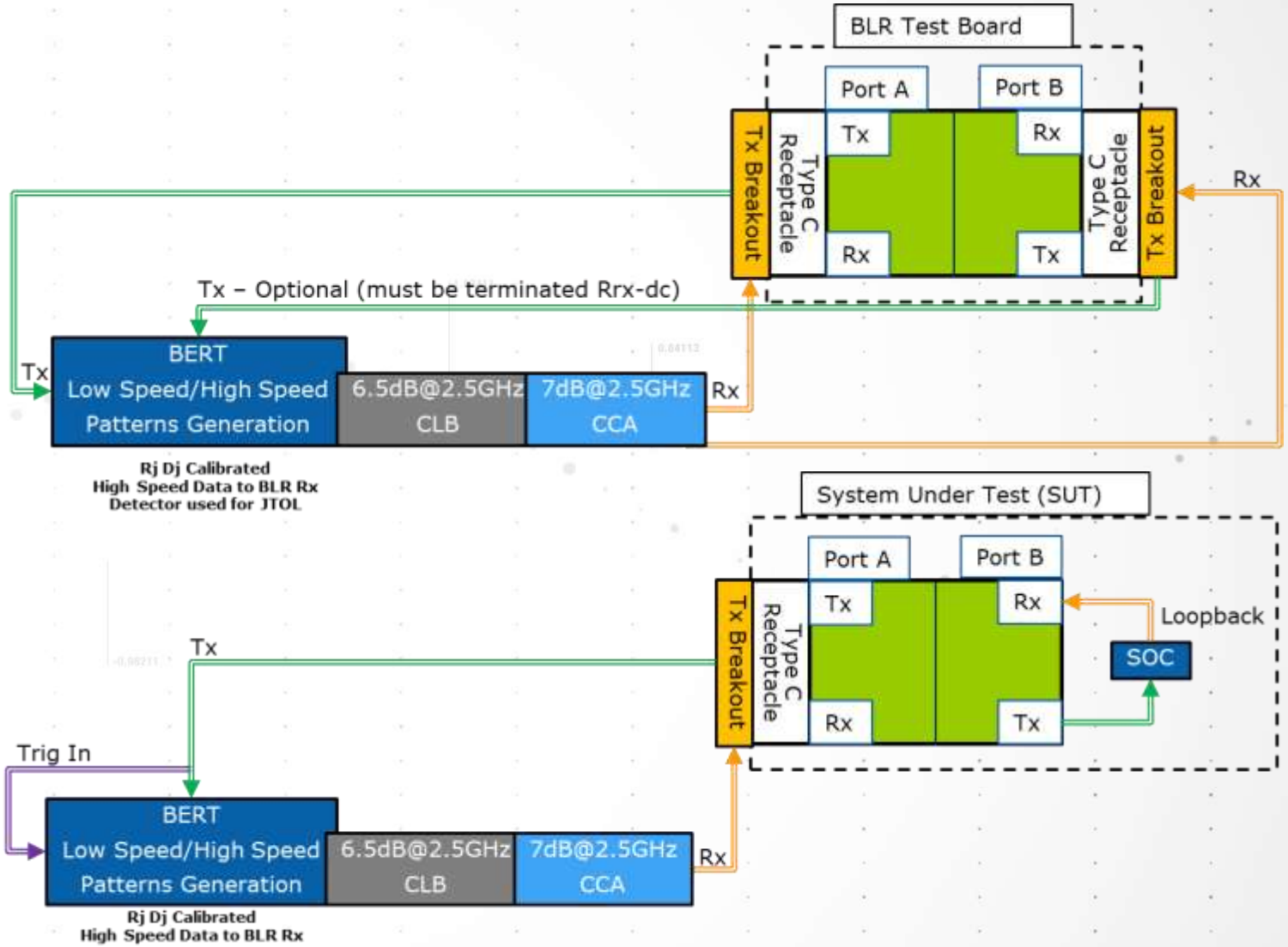
Table E-3. Bit-Level Re-timer Jitter Transfer Function Requirements

Term	Gen 1x1	Notes
Jitter Gain for f<500kHz	0.1dB (max)	Normative requirement.
Jitter Gain for f>500kHz	0.0dB (max)	Normative requirement.



Testing USB 3.2 BLR Retimer RX

- Component
- Embedded
- Pass-through loopback
- Dual-lane symmetrical testing



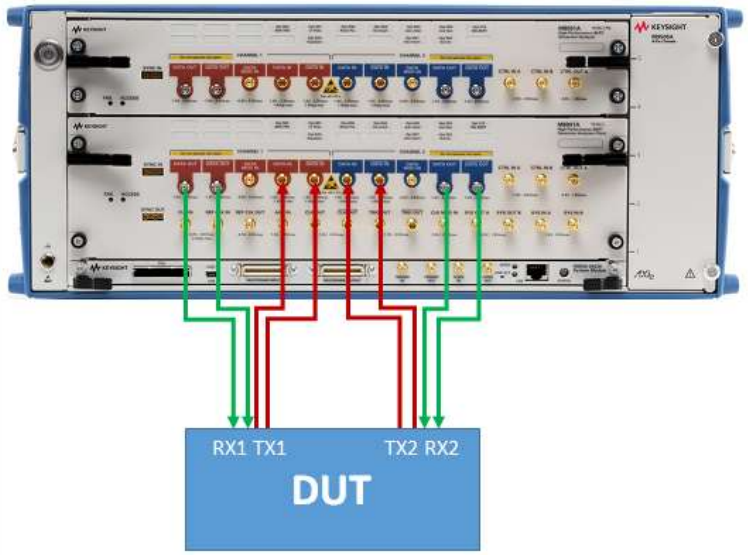
USB 3.2 x2 Test Considerations

Transmitter

- Sufficient bandwidth required on all 4 channels to comprehend crosstalk
- Sufficient bandwidth required on all 4 channels to analyze rise-time and skew
- Updated SW to latest Compliance Test Spec
- Dependencies when coupled with x2 retimers
- Protocol Decode

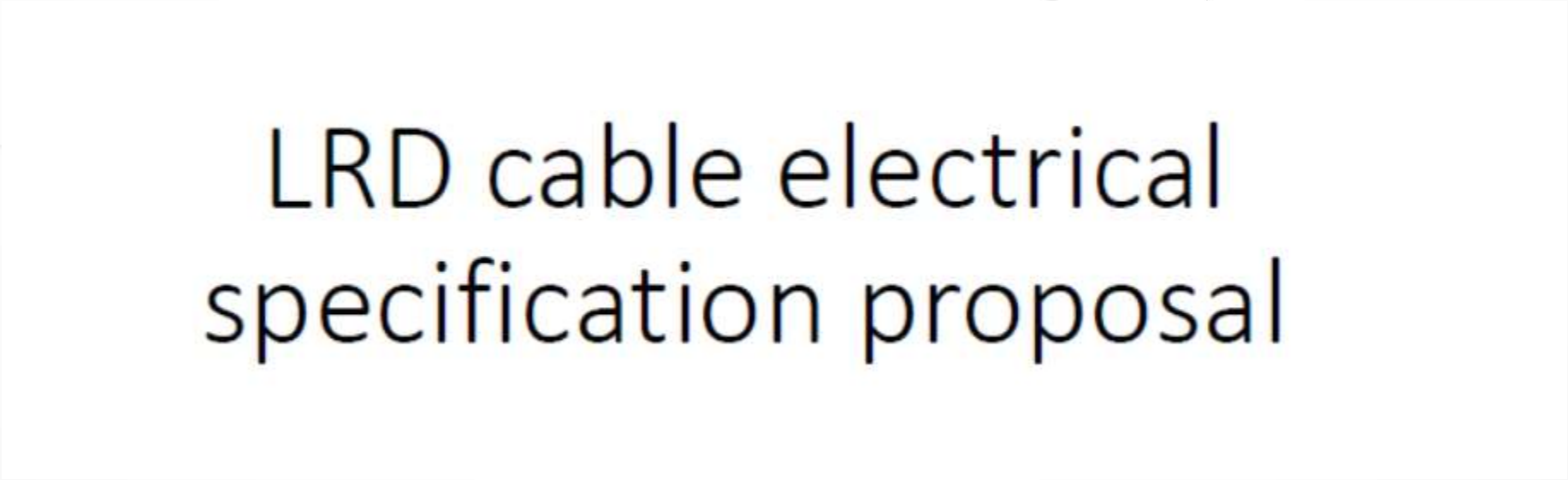
Receiver

- Dual channel Pattern Generator/Error Detector to comprehend crosstalk
- Updated SW to calibrate and test dual channel mode



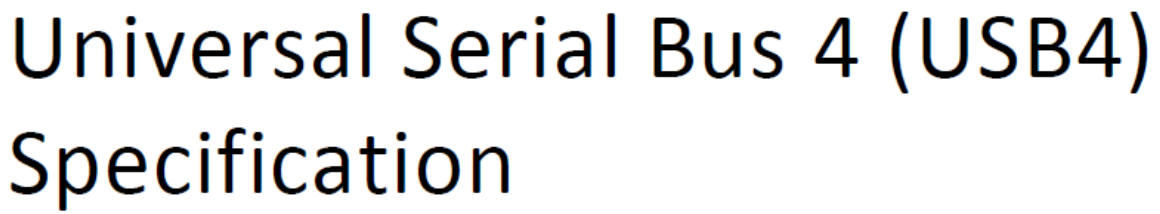
USB 3.2 Cable Redriver Proposal

- Testing as a captive or embedded product
- USB-IF proposing new testing methodology
- Based on Ethernet COM approach



USB4 Overview

- Announced by USB-IF in Q1 2019
- Open standard and integrated in CPU
- Based on the Thunderbolt 3 protocol
- Uses the Type-C connector
- Tunnels USB, DP, and PCIe
- Channel aggregation: two independent 20Gbps bonded into one logical 40Gbps link
- Supports other standards through ALT mode
- Keysight can help test with early adopter Protocol Decode, TX, RX, and Return Loss



USB4 Electrical Testing Methodology

- PHY testing approach will be similar to Thunderbolt 3
  - Tx, Rx, and Return Loss
  - Active and Passive Cable Test

  Plus
  - Type-C Power Delivery
  - DP, USB over Type-C

Universal Serial Bus 4 (USB Type-C)
Electrical Compliance Test Specification

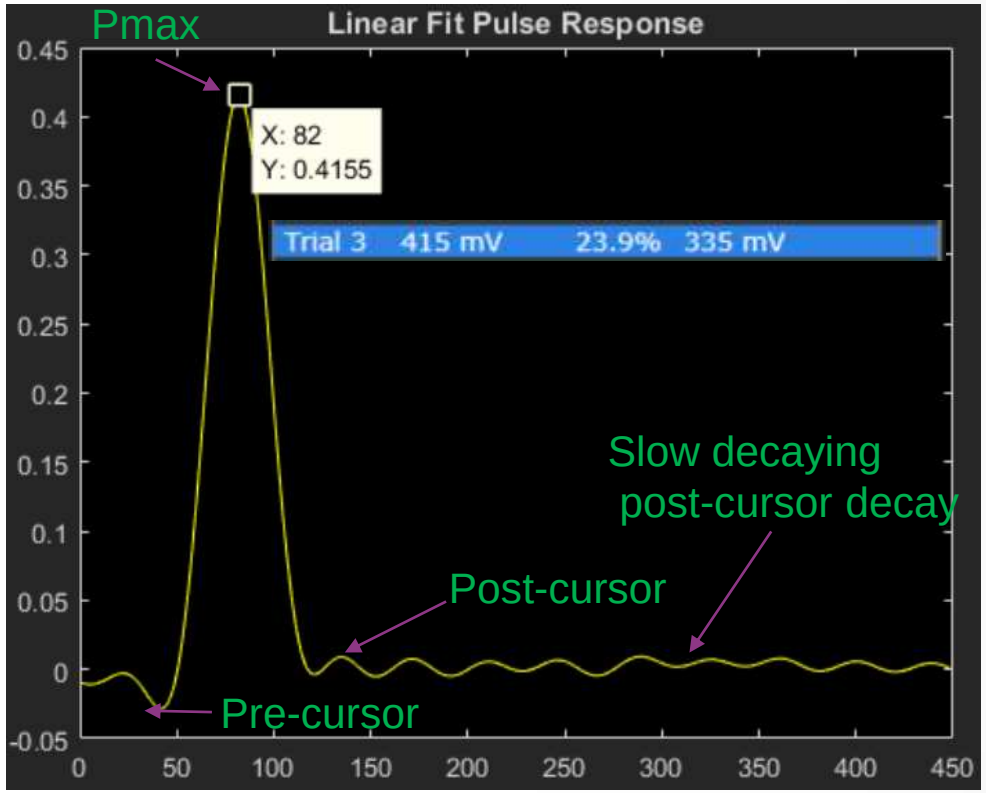
Proposed differences between testing USB 3.2 x1 vs USB4

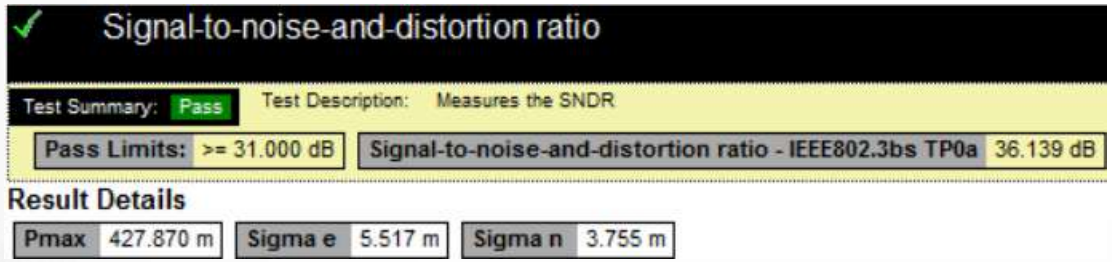
- Return Loss TX and RX
- Transmitter Equalization is not fixed and requires calibration
- Receiver Equalization is much more complex and requires calibration
- PHY bit rate doubles from 10 Gbps to 20 Gbps
- Signaling on all 4 Type-C high-speed pairs
- De-Embedding of Test Cables
- New IL budgets for 10G/20G
- Retimer specific measurements
- Cross-talk Generation
- New Jitter Measurements
- New Phase and Slew Rate Measurements
- Added Skew Measurements
- Common Mode Interference
- Separate Jitter Cocktails for 10G/20G/TP1/TP3EQ
- Link Optimization prior to BER test
- Built in Error Detector

Testing Next-Gen Type-C Standards after USB4 – PAM-4?

PAM-4 Linear Fit Pulse Response and SNDR

- Signal-to-Noise and Distortion Ratio (SNDR)
- P_{max}^2 = Linear Fit Pulse
- σ_e^2 - standard deviation of error
- σ_n^2 - standard deviation of noise
- Peak level is equal to the highest point on the x-axis.
- FIR to address Pre-cursor ISI
- DFE can help post-cursor issues





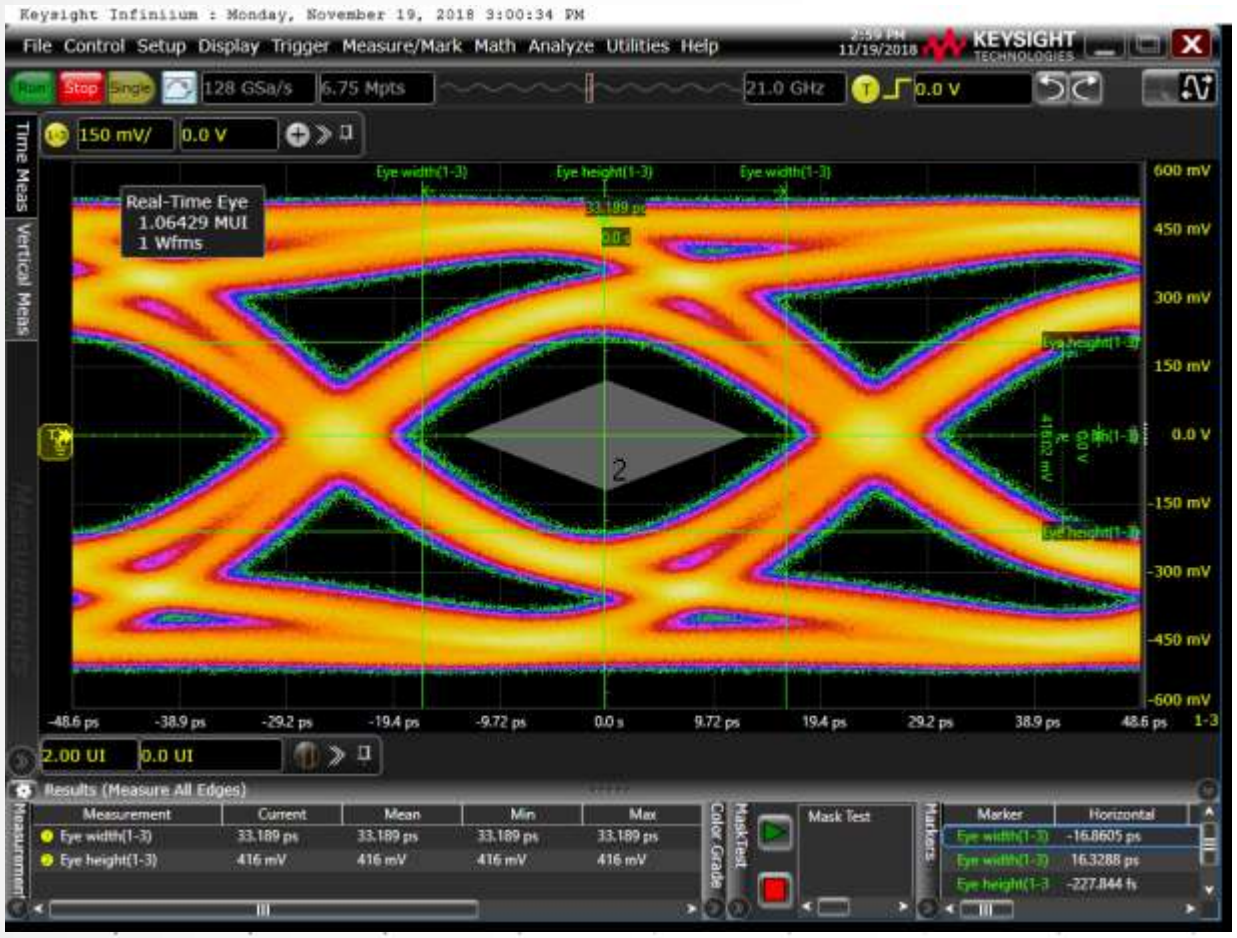
$$SNDR = 10\log_{10}\left(\frac{p_{\max}^2}{\sigma_e^2 + \sigma_n^2}\right)$$

The Industry's Best Signal Integrity

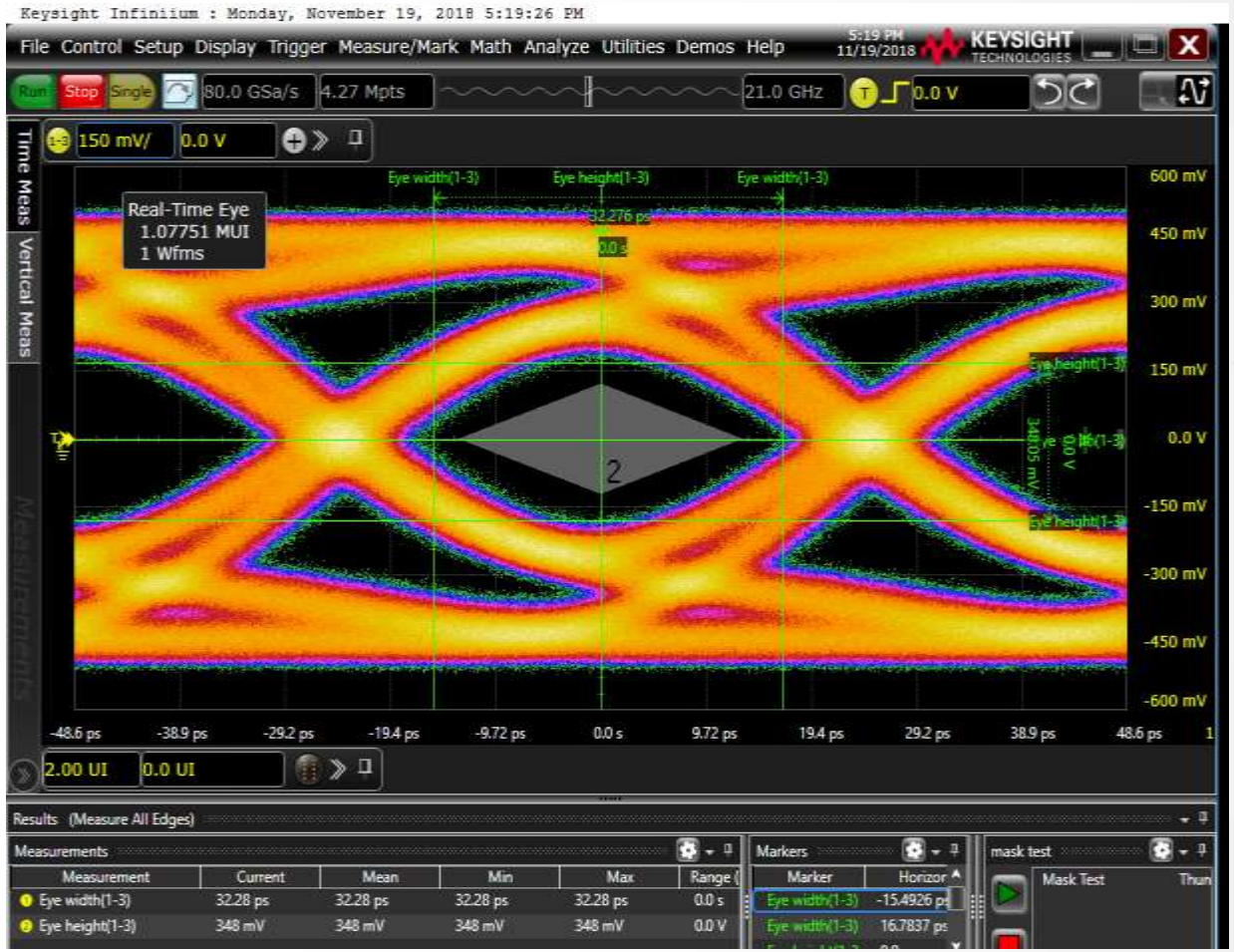
- **Lowest noise**
  < 900 µV rms @ 110 GHz
  < 500 µV rms @ 70 GHz
  < 300 µV rms @ 33 GHz
- **Lowest intrinsic jitter**
  20 fs rms
- **Lowest inter-channel jitter**
  10 fs rms
- **Highest ENOB**
  > 5.0 bits @ 110 GHz
  > 5.4 bits @ 70 GHz
  > 5.9 bits @ 33 GHz
- **Best EVM**
  1.22% for 802.11ay at 61.5 GHz

USB4 Eye (no cable model, no EQ)

UXR series



V series



Eye width = 33.1 ps
Eye height = 416 mV

Eye width = 32.2 ps
Eye height = 348 mV

eUSB2 Protocol Trigger and Decode

- S-Series protocol decode/trigger/search for eUSB2 supports the same features as USB2 decode/trigger/search. No HSIC.
- PID Types: Token, Data, Handshake, Special
- Errors: Any Error, PID Error, 5-bit CRC Error, 16-bit CRC Error, Bit Stuff Error, Glitch
- Additional eUSB2 support for LS/FS Control Messages, Suspend, and Resume
- Can show eUSB2 and USB2 in parallel

Keysight Type-C Test Solution

Design Simulation, Protocol Decode, USB-PD, RF, and Channel Characterization

SW

HW

Fixture

DUT

Transmitter Test
Active Cable Test

Automated Standards Test Software

UXR Infiniium Scope
<1mV RMS
<25fs RMS

N7015A/18A Tx Test Fixture

Tx

Interconnect Test
Return Loss Test

E5071C ENA Option TDR

Cable/Connector Test Fixture

Cable

Receiver Test
Active Cable Test

N5990A Automated Standards Test Software

M8020A Integrated Protocol J-BERT <200fs

N7015A/18A Rx Test Fixture

Tx / Rx

Thank you!
Q/A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